Novel Design of Multiple-Valued Static Memory Array using CNTFET Technology

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Abstract: The conventional Static memory core is extended to achieve multistability (at different operating voltages) without any compromise in the basic cell performance characteristics like wide noise margins, good low voltage stability and low static power consumption. A novel design of SRAM circuit based on quaternary logic and its implementation using Carbon nanotube technology is discussed in this research paper. CNTFETs provide the best path to move ahead from the binary logic paradigm to explore higher logic systems like ternary logic, quaternary logic etc. A 4X4 array of the proposed SRAM cell is created using Row and column address decoders. Read and write functions are demonstrated for every logic data followed by its corresponding power and propagation delay calculations. HSPICE simulations are done and the results are analyzed.

Keywords: Storage cell, CNTFET, VLSI, Static random access memory (SRAM), Multiple-valued logic (MVL), Array, Decoders.

I. INTRODUCTION

For many years, MOSFET was the most basic element of any electronic circuit [1]. In conventional Si-MOSFET, as the gate length reduces to nanometers, short channel effects are observed. One of these effects is direct tunneling between drain and source terminals leading to large variations in parameters. These effects pose difficulty in further scaling the silicon devices. As a result, a lot of effort is being put into trying to adopt the existing Silicon technologies and also overcomes its physical limitations.

Some of the newest technologies are CNTFET (Carbon Nanotube FET), single-electron transistors, silicon-on-insulator, and fin-FETs. With respect to the ballistic transport and also the low OFF-current properties, among these, CNTFET is promising. These properties of the CNTFET enable high-performance while operating at low-power [1]–[6]. The aim of VLSI designers is to meet performance requirements by overcoming the problems associated with physical limits. Further, the famous prophecy of Moore’s law seems to be coming to a standstill with major short channel effects hindering the shrinking of the FET to a large extent which brings in the CNTFET as a possible solution required for the continuous evolution of technology. In particular, CNTFETs make possible the realization of distinct threshold voltages just by the use of different diameters for the carbon nanotubes [7].

Static Random Access Memory (SRAM) is a type of semiconductor memory used to store logical data. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as sufficient power supply voltage is provided), without any need for a periodic refresh operation.

The problems incurred by the conventional binary logic implementations such as high interconnect complexity and low memory density has provided a strong impetus for exploration of multiple-valued logic systems. We seek to combine the potential advantages of these implementations (Multiple-valued logic and CNTFET technology), by designing multivalued SRAM and its 4X4 array to explore beyond-binary and beyond-CMOS logic designs.

The proposed structure of static memory is in congruence with the current fabrication techniques of carbon nanotubes prevalent in the industry. This is mainly because the physical characteristics of every CNTFET inverter unit are the same, but operated at different voltage rails. It is very difficult to fabricate CNTs with unique chiralities and a different number of tubes thus our design can be used to achieve multiple stabilities without compromising any of the perks of the basic cell.

This paper is arranged in the following manner: section II describes different types of CNTFETs and its structures. Section III shows the Quaternary logic implementation followed by Read/write operations on Section IV. With the Address decoders designed in Section V an array is developed. A conclusion is arrived at in Section VI regarding the performance of the proposed design.

II. TYPES OF CNTFETS & THEIR STRUCTURES

A. Back-gated CNTFETs

Here, the SWCNT acts as channel while two metal electrodes act as drain and source terminals. The back gate is made of a heavily doped silicon wafer. I(on)/I(off) ratios of the order of 10^5 is observed. Challenges such as high parasitic contact resistance, low-drive currents and low trans-conductance_{min} observed in back-gated CNTFETs are overcome using top-gated CNTFETs [4].

B. Top-gated CNTFETs

In Top-gated CNTFET 15-20 nm thick film made of SiO2 forms the gate insulator. The gate is placed above the carbon- nanotube. Reduced threshold voltage, increased drain current, trans-conductance and on/off current ratio are some of the advantages of the top gated CNTFETs over back-gated ones [5].
C. Wrap-around gate CNTFETs

In this type of CNTFETs, the entire circumference of the nanotube is gated. As a consequence of this, the leakage current is reduced and the device on/off ratio is improved. Thus, significant enhancements in the electrical performance of the CNTFETs is observed[6].

D. Suspended CNTFETs:

Here, the nanotube is suspended over a trench. This lessensits contact with substrate and gate oxide. In spite of improving the device performance suspended CNTFETs suffer from fewer options available for material options of gate dielectric: either air or vacuum. Gate bias application leads to the nanotube being pulled closer to the gate. This imposes an upper limit on the amount of gating allowed over the nanotube. For commercial applications, suspended CNTFETs aren’t suitable. However, they are used to study clean nanotube properties[7-11].

The Stanford University CNFET Model is used as the reference working at 7nm technology and instantiated directly into Synopsys HSPICE software.

III. QUATERNARY LOGIC IMPLEMENTATION

A. CNTFET Chirality and threshold voltage

Quaternary logic system encompasses four values from machine level logic implementation. Here 0, 1, 2 and 3 denote quaternary values that are to be stored. The fundamental inversion operation in quaternary logic is:

\[ \bar{x} = 3 - x \tag{1} \]

Static complementary CMOS have several advantages like good performance while consuming low power. There is negligibly small static power dissipation. They are also robust in nature. CNTFETs allow controlling threshold voltage by making changesto the chirality vector/diameter of the carbon nanotube. A change in chirality vector results in a change in the threshold voltage of the CNTFET.

Angle of atom arrangement along the tube determines the behavior of an SWCNT. Based on this, it acts as a conductor or a semiconductor. Chirality vector describes this atom arrangement and is denoted by an integer pair \((n, m)\). A carbon nanotube shows metallic behavior if \(n - m\) is an integer. This isn’t the case, the tube is semiconducting. If the threshold voltage is 0.3V, chirality is indicated as \((19, 0)\). For ternary logic implementation, other threshold voltages of 0.6V and 0.45V are required in addition to 0.3V. This is explained in later sections. The threshold voltage is dependent on the diameter of the CNFET. This relation is described as follows.

\[ D_{\text{CNT}} = \frac{\sqrt{3a_0}}{\pi} \sqrt{n^2 + m^2 + nm} \rightarrow \text{Diameter of CNT} \]

\[ a_0 = 0.142nm \] is the inter-atomic distance between any two neighboring carbon atoms.

The I-V characteristics of CNTFETs are similar in nature to that of MOSFETs. The threshold voltage of any transistor is the minimum voltage that turns it ON. The threshold voltage of the CNTFET is an inverse function of its diameter, i.e.

\[ V_{\text{th}} = \frac{E_g}{2e} = \frac{1}{\sqrt{3eD_{\text{CNT}}} aV_{\pi}} \]

\[ a = 2.49 \text{ Å} \] is the inter-atomic distance and \(V_{\pi} = 3.033\text{ eV}\) is the \(\pi-\pi\) bond energy of carbon. This is with reference to the tight bonding model. \(e\) is unit electron charge, and \(D_{\text{CNT}}\) the diameter of the carbon nanotube. The diameter, chirality and the threshold voltage of the CNFETs are inter-related:

\[ \frac{V_{\text{th1}}}{V_{\text{th2}}} = \frac{D_{\text{CNT1}}}{D_{\text{CNT2}}} = \frac{n2}{n1} \]

Therefore, a threshold voltage of 0.293V can be set by using chirality vectors \((m, n) = (19, 0)\)

B. Inverter Design

Three binary inverters are designed, each operating at different \(V_{DD}\) and \(V_{SS}\) and its operation for appropriate inputs are verified.

\[ \text{Fig.1: Inverters with Different Supply Voltages} \]

The threshold voltages of PCNFET device and NCNFET devices used in the inverters of figure [22] are -0.29V and 0.29V respectively. The voltage transfer characteristics of three inverters are as shown in figure [23].

\[ \text{Fig.2: Voltage Transfer Characteristics of The Inverters} \]

C. Circuit description

The proposed memory cell configuration is shown in Fig.3 in a four-valued form. It is constructed by replicating the four-device unit circuit shown in Fig. 4.
Therefore, we can generalize this basic circuit to multistability. The four-valued cell operates with three ordered supply voltages, i.e., GND < V₁ < V₂ < VDD. A common storage node S is connected to these supply rails and ground via four transmission paths [12].

The inverters operate with the supply levels V₁/GND, V₂/V₁ and VDD/V₂, respectively. This selection of supply levels leads to three different logic threshold voltages VT₁, VT₂ and VT₃ in the order GND < VT₁ < V₁ < VT₂ < V₂ < VT₃ < VDD, as shown above. The stored voltages can be explained as follows:

1) If Vs < VT₁, then the GND = 0V is stored in the cell.
2) If VT₁ < Vs < VT₂, then the V₁ = 0.3V is stored in the cell.
3) If VT₂ < Vs < VT₃, then the V₂ = 0.6V is stored in the cell.
4) If VT₃ < Vs, then VDD = 0.9V is stored in the cell.

Write signal is switched on initially. Din flows via the transmission gate and storage node Vs attains this value. Later even after the write is switched off, we can see that the voltage stays at the storage node. This is due to the connection between Vs and the voltages 0V, V1, V2 or Vdd that is established as a result of the operation of one of the three inverters (described earlier) according to the applied input voltage Din. The stored voltage is sampled by applying a read pulse to the TG. OUT signal retains the initial value which was written by Din.

It can be noted that the stored value can be read even after Din is switched off. The operation of the quaternary SRAM cell for write and read operations of logics 0, 1, 2 and 3 are presented in the figures 5, 6, 7 and 8.

IV. READ/WRITE OPERATIONS

Rapid read/write process is the essence to any memory device. Read and write cycles for the proposed design is discussed here. Data are written into the cell by connecting the storage node S to a D-in line via a transmission gate (TG), which has a low ON-resistance.
C. Selection of a particular cell

A 4X4 quaternary SRAM cell array is designed from the basic quaternary SRAM sub circuit. Figure 12 shows the block diagram of the 4X4 quaternary SRAM cell array designed using CNTFETs. As in the case if the ternary SRAM cell, each cell of the array is accessed using row and column decoders, the circuits of which are as shown in figures 10 and 11.

![Fig. 12: 4X4 SRAM Memory Array](image)

VI. PERFORMANCE ANALYSIS

Single SRAM cell is designed in quaternary logic paradigm using CNTFET technology. The power and delay analysis of static quaternary SRAM is tabulated below. Power dissipation and delay is listed in the table when each data logic is stored.

Propagation delay is defined as the delay between the application of write line (WRT) signal and the time at
which the data is actually written into the storage node (VS) of the quaternary SRAM as shown in the figure 14.

<table>
<thead>
<tr>
<th>CNTFET</th>
<th>Stored data</th>
<th>Voltage (V)</th>
<th>Average Power (W)</th>
<th>Delay (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0.2628 nW</td>
<td>0.2628 nW</td>
<td>2.507 pS</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.10587 nW</td>
<td>0.10587 nW</td>
<td>0.284 pS</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>71.412 pW</td>
<td>71.412 pW</td>
<td>47.36 pS</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1.9386 nW</td>
<td>1.9386 nW</td>
<td>0.1160 pS</td>
</tr>
</tbody>
</table>

Table 1: Quaternary CNTFET Based SRAM

The performance of CNTFET based quaternary SRAM cell is compared with the conventional CMOS quaternary design [11]. The power consumed during the storage of logic 2 is least in both technologies whereas the delay corresponding to the storage of 2 is the highest.

<table>
<thead>
<tr>
<th>CMOS (90 nm)</th>
<th>Stored Data</th>
<th>Voltage (V)</th>
<th>Average Power (W)</th>
<th>Delay (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0 V</td>
<td>8.4 nW</td>
<td>195.13 nS</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.4 V</td>
<td>2.67 nW</td>
<td>7.7218 pS</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.8 V</td>
<td>878 pW</td>
<td>338.94 pS</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1.2 V</td>
<td>3.32 nW</td>
<td>5.4178 nS</td>
</tr>
</tbody>
</table>

Table 2: CMOS based Quaternary SRAM

The delay-power product of the CNTFET design is lesser indicating, it has a faster storage process and is better suited for low power, low voltage applications (consumes lower power during operation).

VII. CONCLUSION

The proposed quaternary design demonstrates the possibility of extending a static flip-flop core to multiple-valued memory applications without compromising technological compatibility or the dissipation-free static operation. The basic cell configuration comprises eight devices for three-level operation and requires four devices more for every additional level. Extension to higher level operation is made possible by:

1) Reducing inverter rail-to-rail voltage down to about one device threshold and
2) Operating transmission devices in the subthreshold mode.

Despite the experimental success of the multiple-valued logic paradigms, it faced tremendous difficulties in the fabrication process due to unique device chiralities etc. The proposed Quaternary structure can be used to overcome the fabrication problems faced by its ternary counterpart.

VIII. REFERENCES

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