Reconfigurable NoC for IoT Based SoCs

Namratha Patil¹, Dr. Vasundhara Patel², Prabhu Bhaiри³
¹²Department of ECE, BMS College of Engineering, Bangalore, ³SeviTech Systems Pvt. Ltd. Bangalore
namratha.udc@gmail.com, vasu.ece@bmsce.ac.in, prabhu.bhairi@sevitechsystems.com

Abstract: Advances in VLSI technology allow us to integrate more processing elements on one chip, creating ever more powerful and diverse systems-on-chip (SoC). Most of these elements are available as IP cores, so the main problem for many designers today is connecting them in an efficient way, maximizing performance and minimizing area and power costs. To cover the complexity of future systems, where thousands and hundreds of heterogeneous cores have to be interconnected, new on-chip communication solutions are being searched. In this context, Networks on Chip (NoCs) have been studied as bus alternative. However, the inclusion of NoCs broad design space increases even more the complexity of design flows. Additionally, today electronic industry demands drastic time to market reduction and improved device diversity. On the other side, reconfigurable devices have had an impressive evolution and they are complex heterogeneous platforms which include a broad variety of embedded cores. These tendencies provide support to the idea of reconfigurable on-chip communication, which can reduce the system design time and permit to adapt their characteristics to currently running applications.

Keywords: Network on Chip (NoC), AMBA AHB, System on Chip (SoC), Internet of Things (IoT).

I. INTRODUCTION

Network on chip or network on a chip (NoC or NOC) is a communication subsystem on an integrated circuit, typically between intellectual property (IP) cores in a system on a chip (SoC). NoC technology uses methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. As semiconductor transistor dimensions shrink and increasing amounts of IP block functions are added to a chip, the physical infrastructure that carries data on the chip and its quality of service begins to crumble.

The IoT based system-on-a-chip (SoC) handles processing, connectivity and sensor interfaces on a single die component. This solution speeds development and time to market.

Network Interface provides a customary interface for effortless integration of new processing. In this paper, the design architecture of Network on-chip uses AMBA-AHB based network interface elements in Network on-chip.

II. AHB

The AHB bus is a system bus used in an AMBA bus system along with Advance Peripheral Bus (APB) - a peripheral interconnect bus that is a simpler version of AHB. The AHB implements the features required for high performance, high clock frequency systems including burst transfers, split transactions, single cycle bus master handover, single clock edge operation, non-tristate implementation and wider data bus configurations.

The components of the network interface are arbiter, multiplexer, decoder and lock handler.

Figure 1: Block Diagram of NOC

A. Arbiter

The AMBA bus specification is a multi-master bus standard. As a result, a bus arbiter is needed to ensure that only one bus master has access to the bus at any particular point in time. Each bus master requests control of the bus, and the arbiter decides which has the highest priority and issues a grant signal accordingly.

Figure 2: Block Diagram of AHB Arbiter

The AHB arbiter consists of sub components, namely

- Split grant masking logic
- Round Robin arbitration scheme
Split Grant Masking

When a split transfer is detected, a single bit in the mask register is cleared, which blocks the bus request input of the split master from reaching the arbitration logic. The master number of the previous master (HmasterPrev) stored by the slave is used to determine which bit of mask to clear. The 4-bit HmasterPrev is decoded into 16-bit version.

![Figure 3: Block Diagram of Split Grant Masking](image)

Round Robin Arbitration Scheme

The round robin arbitration with inputs rst, clk and req is designed which produces output grant. For now, in this design, only two masters are used and so there will be two requests req[0] and req[1] as shown below.

![Figure 4: Block diagram of round robin arbitration](image)

B. Decoder

The system decoder is used to decode the address bus and generate select lines to each of the system bus slaves, indicating that a read or write access to that slave is required. Figure below shows the decoder module interface block diagram.

![Figure 5: Block Diagram of Decoder](image)

C. Multiplexor

Master to Slave Multiplexor

The master to slave multiplexor is used to connect all of the system bus masters to the bus slaves, using the current HMASTER number to select the bus master outputs to use. It is also used to generate the default master outputs when no other masters are selected. Figure below shows an interface diagram of the master to slave multiplexer module.

![Figure 6: Block Diagram of Master to Slave Multiplexer](image)

III. PROPOSED WORK OF RECONFIGURABLE NOC FOR IOT BASED SOCS

In this paper, the design architecture of Network on-chip is using AMBA-AHB based network interface. In existing work, they can design a NoC architecture for fixed number of masters and slaves. But here the proposed is to design a reconfigurable network on-chip communication using AMBA protocol to reduce the system design time and permit to adapt their characteristics to currently running applications.

IV. EXPERIMENTAL RESULTS AND VERIFICATION

The simulation results of the decoder are shown below.
V. CONCLUSION

In this paper, the architecture of NOC with Network Interface (NI) as AMBA AHB is implemented. We can also implement this architecture of NOC using AXI protocol for improved system performance. Based on this concept of reconfigurable NOC, we are going to design a NOC with network element based on AXI protocol as future work to accomplish low power consumption and high speed which can improve the system performance.

VI. REFERENCES


