A Single-Phase Grid Connected Photovoltaic Power Generation System Using Seven-Level Inverter and Modified DC-DC Power Converter

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Abstract: Applications with photovoltaic (PV) energy have rapidly increased in response to concerns about global climate change and energy sources. This paper proposes a Single-phase grid-connected seven-level inverter and a modified dc-dc power converter for Photovoltaic power generation system. The circuit consists of a dc/dc power converter and a seven-level inverter. The dc/dc power converter combines the dc–dc boost converters and a transformer to convert the output voltages of PV cell array into two independent voltage sources with multiple relationships. The seven-level inverter is capable of producing seven levels of output voltage. Thus, the PV power generation system generates a sinusoidal output current in reference to the grid voltage. The salient features of the proposed seven-level inverter are that only six power electronic switches are used, and only one power electronic switch is switched at high frequency at any time.

Key Words: Grid-connected, multilevel inverter, boost converter.

I. INTRODUCTION

Photovoltaics allow the consumers to generate electricity in a clean, reliable and quiet manner. Photovoltaics are often abbreviated as PV. Photovoltaic cells combine to form photovoltaic systems. Photovoltaic cells are devices that convert light energy or solar energy into electricity. As the source of light is usually the sun, they are often referred to as solar cells. The word photovoltaic is derived from “photo,” meaning light, and “voltaic,” which refers to production of electricity. Hence photovoltaic means “production of electricity directly from sunlight.” Usually, a PV system is composed of one or more solar PV panels, an AC/DC power converter (also known as an inverter), and a rack system that holds the solar panels, and the mountings and connections for the other parts. A small PV system can provide energy to a single consumer, or to isolated devices like a lamp or a weather device. Large grid-connected PV systems can provide the energy needed to serve multiple customers.

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The power conversion interface is important to grid connected solar power generation systems because it converts the dc power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the dc power to ac power. Since the output voltage of a solar cell array is low, a dc–dc power converter is used in a small-capacity solar power generation system to boost the output voltage, so it can match the dc bus voltage of the inverter.

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A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW[3]. Types of single-phase grid-connected inverters have been investigated. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter’s switching operation. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped [7]-[11], flying capacitor or multi cell [12]-[14], cascaded H-bridge [15]-[18], and modified H-bridge multilevel. This paper recounts the development of a solar power generation system which is composed of a dc/dc power converter and a seven-level inverter. The seven-level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascade. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Since only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage, the switching power loss is reduced, and the power efficiency is improved.

II. PHOTOVOLTAIC ARRAY MODELLING

Photovoltaic (PV) cells, or solar cells, take advantage of the photoelectric effect to produce electricity. The building blocks of all PV systems are PV cells because they are the devices that convert solar energy into electrical energy.
Usually known as solar cells, individual PV cells are electricity-producing devices made of semiconductor materials. PV cells come in many sizes and shapes, from smaller than a postage stamp to several inches across. They are more often than not connected together to form PV modules that may be up to several feet long and a some feet wide.

The solar cell arrays or PV arrays are usually constructed out of small identical building blocks of single solar cell units. They determine the rated output voltage and current that can be drawn for some given set of atmospheric data. The rated current is given by the number of parallel paths of solar cells and the rated voltage of the array is dependent on the number of solar cells connected in series in each of the parallel paths.

A solar cell is basically a p-n junction fabricated in a thin substrate of semiconductor. When exposed to sunlight, some electron-hole pairs are created by photons that carry energy higher than the band-gap energy of the semiconductor. The figure shows the typical equivalent circuit of a PV cell.

Fig 1 PV cell single diode equivalent circuit diagram

The typical I-V output characteristics of a PV cell are shown by the following equations:

Module Photo current ($I_{ph}$):

$$I_{ph} = [I_{sc} + K_T(T - 298)]G/1000$$

Module reverse saturation current ($I_{rs}$):

$$I_{rs} = \frac{I_{sc}}{e^{\frac{qV_{oc}}{n_AK_T}}} - 1$$

Module saturation current ($I_o$):

$$I_o = I_{rs} = \frac{T_r}{T} e^{\frac{qE_{go}}{kT_r}}$$

The current output of PV module ($I_c$):

$$I_c = N_pI_{ph} - N_I \left[ e^{\frac{q(V_c + I_{ph})}{n_AK_T}} - 1 \right]$$

where

- $V_c$ is output voltage of PV module(V)
- $T_r$ is the reference temperature = 289K
- $T$ is the module operating temperature
- $A$ is an ideality factor = 1.6
- $K$ is Boltzmann constant = 1.3805 * 10^-23 J/K
- $q$ is electron charge
- $R_s$ is the series resistor of PV module
- $I_{sc}$ is the PV module short circuit current = 1.1A
- $K$ is the short circuit current temperature coefficient=0.0017A/C
- $G$ is the PV module illumination = 1000W/m2
- $E_{go}$ is the band gap for silicon = 1.1eV
- $V_o$ is the open circuit voltage = 18V

III. CIRCUIT CONFIGURATION

Fig. 1. Configuration of the proposed solar power generation system.

The proposed photovoltaic power generation system is composed of a photovoltaic array, a dc–dc power converter, and a new seven-level inverter. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. The dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance $L_f$ was used to filter the current injected into the grid.

The seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, connected in a cascade. The capacitor selection circuit outputs a three-level dc voltage by proper selection of capacitors. The power electronic switches of capacitor selection circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in series. The full-bridge power converter further converts this three-level dc voltage to a seven-level ac voltage that is synchronized with the utility voltage.
IV. DC–DC POWER CONVERTER

The dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. The dc–dc power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven-level inverter.

![Image](https://example.com/image)

Fig. 2. Operation of dc–dc power converter: (a) $S_{D1}$ is on and (b) $S_{D2}$ is off.

The boost $L_D$ converter is composed of an inductor $L_D$, a power electronic switch $S_{D1}$, and a diode, $D_{D1}$. The boost converter charges capacitor $C_2$ of the seven-level inverter. An inductor $L_D$, power electronic switches $S_{D1}$ and $S_{D2}$, a transformer, and diodes $D_{D1}$ and $D_{D2}$ charges capacitor $C_1$ of the seven-level inverter.

When $S_{D1}$ is turned ON as shown in Fig. 3, the PV array supplies energy to the inductor $L_D$. When $S_{D1}$ is turned OFF and $S_{D2}$ is turned ON, its operating circuit is shown in Fig. 2(b). Accordingly, capacitor $C_1$ is connected to capacitor $C_2$ in parallel through the transformer, so the energy of inductor $L_D$ and the solar cell array charge capacitor $C_2$ through $D_{D1}$ and charge capacitor $C_1$ through the transformer and $D_{D1}$ during the off state of $S_{D1}$. Since capacitors $C_1$ and $C_2$ are charged in parallel by using the transformer, the voltage ratio of capacitors $C_1$ and $C_2$ is the same as the turn ratio (2:1) of the transformer. Therefore, the voltages of $C_1$ and $C_2$ have multiple relationships. The boost converter is operated in the continuous conduction mode (CCM). The voltage of $C_2$ can be represented as

$$V_{c2} = \frac{1}{1-D} V_s$$

where $V_s$ is the output voltage of solar cell array and $D$ is the duty ratio of $S_{D1}$. The voltage of capacitor $C_1$ can be represented as

$$V_{c1} = \frac{1}{2(1-D)} V_s$$

in the proposed dc–dc power converter, the energy stored in the magnetizing inductance is delivered to capacitor $C_2$ through $D_{D2}$ and $S_{D1}$ when $S_{D2}$ is turned OFF. Since the energy stored in the magnetizing inductance is transferred forward to the output capacitor $C_2$ and not back to the dc source, the power efficiency is improved. In addition, the power circuit is simplified because the charging circuits for capacitors $C_1$ and $C_2$ are integrated. Capacitors $C_1$ and $C_2$ are charged in parallel by using the transformer, so their voltages automatically have multiple relationships. The control circuit is also simplified.

V. SEVEN-LEVEL INVERTER

The proposed single-phase seven-level inverter comprises a single-phase full-bridge power converter, two bidirectional switches for capacitor selection. The operation of the seven level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are assumed to be ideal, while the voltages of both capacitors $C_1$ and $C_2$ in the capacitor selection circuit are constant and equal to $V_{dc}/3$ and $2V_{dc}/3$, respectively. Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility voltage, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. Proper switching of the inverter can produce seven output voltage levels $V_{dc}$, $2V_{dc}/3$, $V_{dc}/3$, $0$, $-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$ from the dc supply voltage. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Fig. 3.

![Image](https://example.com/image)

Fig. 3. Operation of the seven-level inverter in the positive half cycle, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.
Mode 1: The operation of mode 1 is shown in Fig. 3(a). Both $S_{c1}$ and $S_{c2}$ of the capacitor selection circuit are OFF, so $C_1$ is discharged through $D_1$ and the output voltage of the capacitor selection circuit is $V_{dc}/3$. $S_1$ and $S_4$ of the full bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is $V_{dc}/3$.

Mode 2: The operation of mode 2 is shown in Fig. 3(b). In the capacitor selection circuit, $S_{c1}$ is OFF and $S_{c2}$ is ON, so $C_2$ is discharged through $S_{c2}$ and $D_2$ and the output voltage of the capacitor selection circuit is $2V_{dc}/3$. $S_1$ and $S_4$ of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is $2V_{dc}/3$.

Mode 3: The operation of mode 3 is shown in Fig. 3(c). In the capacitor selection circuit, $S_{c1}$ is ON. Since $D_2$ has a reverse bias when $S_{c1}$ is ON, the state of $S_{c2}$ cannot affect the current flow. Therefore, $S_{c2}$ may be ON or OFF, to avoiding switching of $S_{c2}$. Both $C_1$ and $C_2$ are discharged in series and the output voltage of the capacitor selection circuit is $V_{dc}$. $S_1$ and $S_4$ of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is $V_{dc}$.

Mode 4: The operation of mode 4 is shown in Fig. 3(d). Both $S_{c1}$ and $S_{c2}$ of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is $V_{dc}/3$. Only $S_4$ of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the antiparallel diode of $S_2$ to be switched ON for continuous conduction of the filter inductor current. At this point, the output voltage of the seven level inverter is zero.

Therefore, in the positive half cycle, the output voltage of the seven-level inverter has four levels: $V_{dc}$, $2V_{dc}/3$, $V_{dc}/3$, and $0$.

In the negative half cycle, the output current of the seven-level inverter is negative. The operation of the seven-level inverter can also be further divided into four modes, as shown in Fig. 4. A comparison with Fig. 3 shows that the operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that $S_2$ and $S_3$ of the full-bridge power converter are ON during modes $5$, $6$, and $7$, and $S_2$ is also ON during mode $8$ of the negative half cycle. Accordingly, the output voltage of the capacitor selection circuit is inverted by the full-bridge power converter, so the output voltage of the seven-level inverter also has four levels: $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, and $0$.

In the positive half cycle, when the utility voltage is smaller than $V_{dc}/3$, the seven-level inverter must be switched between modes $1$ and $4$ to output a voltage of $V_{dc}/3$ or $0$. Within this voltage range, $S_1$ is switched in PWM. The duty ratio $d$ of $S_1$ can be represented as

$$d = \frac{V_m}{V_{tri}}$$

where $V_m$ and $V_{tri}$ are the modulation signal and the amplitude of carrier signal in the PWM circuit, respectively. The output voltage of the seven-level inverter can be written as

$$V_o = d \frac{V_m}{V_{tri}} = K_{pwm} \frac{V_m}{V_{tri}}$$

where $K_{pwm}$ is the gain of inverter, which can be written as

$$K_{pwm} = \frac{V_{dc}}{3V_{tri}}$$

When the utility voltage is smaller than $V_{dc}/3$ the seven-level inverter is switched between modes $2$ and $1$, in order to output a voltage of $2V_{dc}/3$ or $V_{dc}/3$ when the utility voltage is in the range ($V_{dc}/3$, $2V_{dc}/3$). Within this voltage range, $S_{c2}$ is switched in PWM. However, the output voltage of seven-level inverter can be written as

$$V_o = d \frac{V_{dc}}{3} + \frac{V_{dc}}{3} = K_{pwm} \frac{V_m}{V_{tri}} + \frac{V_{dc}}{3}$$

The seven-level inverter is switched between modes $3$ and $2$ in order to output a voltage of $V_{dc}$ or $2V_{dc}/3$, when the utility voltage is in the range ($2V_{dc}/3$, $V_{dc}$). Within this voltage range, $S_{c1}$ is switched in PWM and $S_{c2}$ remains in
the ON state to avoid switching of \( s_{s2} \). However, the output voltage of seven-level inverter can be written as

\[
V_o = d \frac{V_{dc}}{3} + 2 \frac{V_{dc}}{3} = K_{pv} \cdot V_m + 2 \frac{V_{dc}}{3}
\]

In the negative half cycle, the seven-level inverter is switched between modes 5 and 8, in order to output a voltage of \(-V_{dc}/3\) or 0, when the absolute value of the utility voltage is smaller than \(V_{dc}/3\). Accordingly, \( s_3 \) is switched in PWM. The seven level inverter is switched in modes 6 and 5 to output a voltage of \(-2V_{dc}/3\) or \(-V_{dc}/3\) when the utility voltage is in the range \((-V_{dc}/3, -2V_{dc}/3)\). Within this voltage range, \( s_{s2} \) is switched in PWM. The seven-level inverter is switched in modes 7 and 6 to output a voltage of \(-V_{dc}\) or \(-2V_{dc}/3\), when the utility voltage is in the range \((-2V_{dc}/3, -V_{dc})\). At this voltage range, \( s_{s1} \) is switched in PWM and \( s_{s2} \) remains in the ON state to avoid switching of \( s_{s2} \).

### Table 1. States of Power Electronic Switches For a Seven-Level Inverter

<table>
<thead>
<tr>
<th>Positive Half Cycle</th>
<th>( S_{s1} )</th>
<th>( S_{s2} )</th>
<th>( S_1 )</th>
<th>( S_2 )</th>
<th>( S_3 )</th>
<th>( S_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(</td>
<td>V_u</td>
<td>&lt; V_{dc}/3 )</td>
<td>off</td>
<td>off</td>
<td>PWM</td>
<td>off</td>
</tr>
<tr>
<td>( 2V_{dc}/3 )</td>
<td>off</td>
<td>PWM</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>(</td>
<td>V_u</td>
<td>&gt; 2V_{dc}/3 )</td>
<td>pwm</td>
<td>on</td>
<td>on</td>
<td>off</td>
</tr>
</tbody>
</table>

| Negative Half Cycle | \( |V_u| < V_{dc}/3 \) | off | off | off | PWM | off |
|---------------------|------------------|------|------|-----|------|------|
| \( 2V_{dc}/3 \) | off | PWM | off | on | off | on |
| \( |V_u| > 2V_{dc}/3 \) | pwm | on | on | on | off | off |

### VI. PV INVERTER POWER STAGE PARAMETERS DESIGN

In designing the power stage of the inverter there are important parameters needed to be considered in the design process. In the input stage, the input voltage range, nominal output voltage and maximum output current. In the output stage the filter is essential. In the design some of the assumptions are needed to compromise the design.

**Input Inductance \( L_D \):** In most designs, the inductor is always given in a certain range provided in the data sheet. However it is wise to estimate the boost inductor directly if no data sheet available. The estimation is calculated using equation [19]

\[
L_D = \frac{V_{pv} \cdot (V_{out} - V_{pv})}{\Delta I_L \cdot V_{out} \cdot f_s}
\]

Where:

- \( \Delta I_L \) = Estimated inductor ripple current
- \( f_s \) = Switching frequency

\( V_{out} \) = Desired output voltage

\( L_D \) = Boost or PV input inductor

\( V_{pv} \) = Typical input voltage

The inductor ripple current can be estimated by 20% to 40% of the output maximum current.

\[
\Delta I_L = 0.2 \cdot I_{out,max} \cdot \frac{V_{out}}{V_{pv}}
\]

**Input capacitance \( C_{pv} \):** In practice, the large current ripple of DC inductor or boost inductor will lead to the significant voltage oscillation in PV panel when input capacitance filter is not connected. This inductor is small normally assumed in high frequency switching converter to reduce the system cost and size. With a small filter or input capacitor added, the voltage ripple across PV panel can be reduced significantly. The input capacitance is very much depends on the IV characteristics of the PV array at MPPT. The capacitors are placed in parallel with the PV array.

The input capacitance is then estimated as:

\[
C_{pv} = \frac{D \cdot V_{pv}}{4 \cdot f_s^2 \cdot L_d \cdot \Delta V_{pv}}
\]

duty ratio \( D = 1 - \frac{V_{pv}}{V_{out}} \)

In the variation of temperature and irradiance, the capacitance will see the voltage ripple from the PV array MPP as \( \Delta V_{pv} \).

**DC Link Capacitor \( C_2 \):** The DC link capacitor \( C_2 \) is sized according to the equation[20][21]

\[
C_2 = \frac{P_{pv}}{2 \cdot \omega \cdot V_{DC} \cdot \sqrt{V}}
\]

Where the ripple voltage \( \sqrt{V} \) is taken as 10% of the specified bus voltage or link voltage and \( \omega \) is the grid frequency. \( P_{pv} \) is the nominal power from the strings.

**L-C-L Filter Design:** The main function of the LCL filter is to reduce high-order harmonics on the output side; however poor design may cause a distortion increase. Therefore, the filter must be designed correctly and reasonably.
The value of the ripple output current is used in estimating the value of the inverter side inductance: \( L_i \)

\[
L_i = \frac{V_{DC}}{16 * f_e * \nabla I_L}
\]

Where \( f_e \) is the switching frequency and the output ripple current \( \nabla I_L \) is 10% of the rated output current.

\[
\nabla I_L = 10% * \frac{\sqrt{2} * P_N}{V_{phase.grid}}
\]

Where \( P_N \) is the output power of the Inverter and \( V_{phase.grid} \) is the grid voltage.

Inverter inductance \( L_i \) and grid inductance \( L_g \) are related with \( r \) in equations below. If 5% is taken as attenuation factor of the filter, then the approximated value of \( r \) is 0.6

\[
L_g = r * L_i
\]

The filter capacitance \( C_f \) of the L-C-L filter is limited to 5% of the rated output power. Usually is taken as the fraction of the base capacitance, \( C_b \)

\[
C_f = 5% * C_b = 0.05 * \frac{P_N}{\omega_{grid} * V_{phase.grid}}
\]

The passive damping resistor \( R_d \), is obtained at the resonance frequency \( f_o \) of the L-C-L filter. The values of damping resistance and resonance frequency are given in the equations 4.13 and 4.14

\[
R_d = \frac{1}{3 * \omega_o * C_f}
\]

\[
f_o = \frac{1}{2\pi} * \frac{L_i + L_g}{\sqrt{L_i * L_g * C_f}}
\]

VII. CONTROL BLOCK

The proposed solar power generation system consists of a dc–dc power converter and a seven-level inverter. The seven-level inverter converts the dc power into high quality ac power and feeds it into the utility and regulates the voltages of capacitors \( C_1 \) and \( C_2 \). The dc–dc power converter supplies two independent voltage sources with multiple relationships and performs maximum power point tracking (MPPT) in order to extract the maximum output power from the solar cell array.

The above figure shows the control block diagram for the dc–dc power converter. Dual control loops, an outer voltage control loop and an inner current control loop, are used to control the dc–dc power converter. The outer voltage control loop is used to regulate the output voltage of the PV array. The inner current control loop controls the inductor current so that it approaches a constant current and blocks the ripple voltages in \( C_1 \) and \( C_2 \). The Incremental conductance method is used to provide MPPT. The output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage for the solar cell array. The PWM circuit generates a set of complementary signals that control the power electronic switches of the dc–dc power converter.

Fig. 8 shows the control block diagram for the seven-level inverter. The utility voltage is detected by a voltage detector, and then sent to a phase-lock loop (PLL) circuit in order to generate a sinusoidal signal with unity amplitude. The voltage of capacitor \( C_2 \) is detected and then compared with a setting voltage. The compared result is sent to a PI controller. Then, the outputs of the PLL circuit and the PI controller are sent to a multiplier to produce the reference signal, while the output current of the seven-level inverter is detected by a current detector. The reference signal and the detected output current are sent to absolute circuits and then sent to a subtractor, and the output of the subtractor is sent to a current controller. The absolute utility voltage is also sent to an absolute circuit and then sent to a comparator circuit, where the absolute utility voltage is compared with both half and whole of the detected voltage of capacitor \( C_2 \), in order to determine the range of the operating voltage. The comparator circuit has three output signals, which correspond to the operation voltage ranges, (0, \( V_{dc}/3 \)), (\( V_{dc}/3 \), \( 2V_{dc}/3 \)), and (\( 2V_{dc}/3 \), \( V_{dc} \)). The feed-forward control eliminates the disturbances of the utility voltage. The absolute value of the utility voltage and the outputs of the compared circuit are sent to a feed-forward controller to generate the feed-forward signal. Then, the output of
the current controller and the feed-forward signal are summed and sent to a PWM circuit to produce the PWM signal. The detected utility voltage is also compared with zero, in order to obtain a square signal that is synchronized with the utility voltage. Finally, the PWM signal, the square signal, and the outputs of the compared circuit are sent to the switching signal processing circuit to generate the control signals for the power electronic switches of the seven-level inverter, according to Table I.

VIII. ANALYSIS

Since only six power electronic switches are used in the proposed seven-level inverter, the power circuit is significantly simplified compared with a conventional seven-level inverter. The states of the power electronic switches of the seven-level inverter, as detailed previously, are summarized in Table I. It can be seen that only one power electronic switch is switched in PWM within each voltage range and the change in the output voltage of the seven-level inverter for each switching operation is \( V_{dc}/3 \), so switching power loss is reduced. Figs. 3 and 4 show that only three semiconductor devices are conducting in series in modes 1, 3, 4, 5, 7, and 8 and four semiconductor devices are conducting in series in modes 2 and 6. This is superior to the conventional multi-level inverter topologies, in which at least four semiconductor devices are conducting in series. Therefore, the conduction loss of the proposed seven-level inverter is also reduced slightly. The drawback of the proposed seven-level inverter is that the voltage rating of the full-bridge converter is higher than that of conventional multilevel inverter topologies. The drawback of the proposed seven-level inverter is that the voltage rating of the full-bridge converter is higher than that of conventional multilevel inverter topologies.

In order to supply the grid with a sinusoidal line current without harmonic distortion, the inverter is connected to the supply network via filter. The filter is an important part of every semiconductor converter. The filter reduces the effects caused by switching semiconductor devices on other devices.

The main functions of filter includes convert the voltages from switch devices to current, to reduce high frequency (HF) switching noises and protect the switching devices from transients. The L-C-L filter has good current ripple attenuation even with small inductance values.

IX. SIMULATION RESULTS

The performance of the proposed converter and the control strategy are evaluated by conducting the Simulation analysis of the system using MATLAB/Simulink version R2013a. MATLAB is a high-level language and interactive environment that facilitates to perform computationally intensive tasks faster than with traditional programming languages such as C, C++, and Fortran. Simulink® is an environment for multi-domain simulation and model-based design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that enables to design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing etc.
Simulation is performed using PV array with output voltage of 45V. The seven-level inverter is connected to a grid voltage of 210V with frequency of 50Hz. The output voltage of inverter is of seven level as shown in fig(14). It is shown that the output voltage of inverter is in phase with grid voltage.

Fig.14 Inverter switching pulses

X. CONCLUSION

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a seven-level inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Simulation results show that the proposed solar power generation system generates a seven-level output voltage. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell array.

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XI. REFERENCES


