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Design & Simulation of Dynamic UART Using Scan Path Technique (USPT)

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Abstract: ***This paper presents design and simulation of Universal Asynchronous Receiver and Transmitter (UART) using Scan path Technique (SPT). The main focus is on simulation and optimization of UART design and computing its speed of operation. The design of UART using SPT is better than the other previous design in terms of LUT's (number of gates), complexity, size and cost. This design is operated at the maximum Frequency of 151.446 MHz and using only 22 LUT's Blocks as compared to 109 by one and 90 by other one in. Where as in percentage it uses only 9% of LUT's and without using FSM as compared to 49% of LUT's are used by one and 42% of LUT's are used by others. In this research paper a novel UART is presented using SPT which fairly improves its performance and makes the design efficient with respect to conventional designs.. The device converts incoming parallel data signal to serial data signal which can further sent on a communication transmissions lines. The simulation and designing of UART has been done on Xilinx v 14.5 software packages using Very High Speed Integrated circuit hardware description language (VHDL).***

Keywords: Scan path technique, universal asynchronous receiver and transmitter (UART), Look up tables (LUT's), parity checking, RTL, FSM, VHDL

I. INTRODUCTION

A Universal asynchronous receiver /transmitter (UART) is an integrated circuit which play a vital role in serial communication [1]. It helps to convert between serial and parallel data. The Serial Communication helps to minimize the distortion of a signal, therefore makes the data transfer between two systems separated in great distance possible.

The transmission of digital information in form of bits through a single wire is easier than parallel transmission through multiple wires. The UART allows the devices to communicate without any synchronization.

UART must have internal buffer to store data coming from the modem until the CPU has time to process it. The serial transmission module is divided into three sub modules: Transmitter, Receiver, and Baud rate generator [2]. Therefore the implementation or realization of UART module is simply communicating with the three sub- modules.

The Receiver module receives the digital information (bits) in serial form at receiving end (RXD) and converts them into parallel data. The Transmitter module converts the bytes into serial bits at transmitter (TXD) end. This design of UART component is built in HDL designing techniques [3].

A UART is an integrated circuit compile with programming that control the computer interface to attached serial devices.

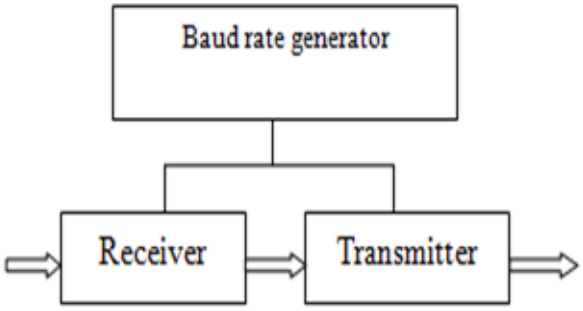

Fig.1 UART Module

It provides the system with Max-232 data terminal equipment (DTE). [4]

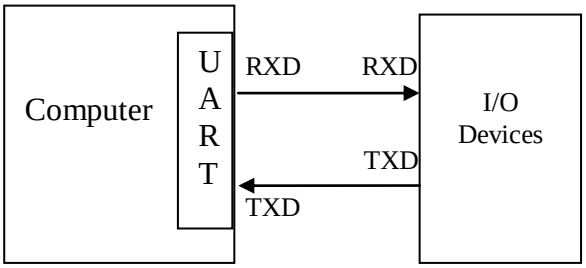

Fig2.Handshaking between I/O devices

II. SERIAL DATA TRANSMISSION

The communication through computers, talk to one another may be either serial or parallel. A parallel communication or links transmits several streams of data along multiple channels.

1. A serial connection requires less number of interconnecting cables (e.g. wires/fibers).
2. An issue of crosstalk is less, because the serial data transfer uses fewer pins.

Why Serial Data Transfer?: Serial cables can be longer than parallel. The serial port transmits a '1' as -3 to -25 volts and '0' as +3 to +25 volts. Whereas parallel port transmit a '0' as 0 volts and '1' as 5 volts [5]. The maximum of 50 volts can generate in serial communication than parallel which has a maximum of 5volts. Therefore cable loss is not going to be more problems for serial cables then they are for parallel. And also, there is no need of large numbers of cables for parallel transmission. If our device needs to be

mounted a far distance away from the computer then three cores cable is going to be a lot cheaper than running nineteen or twenty-five cores cables in parallel communication.

Synchronous Serial Transmission: Synchronous serial transmission requires the Tx (Transmitter) and Rx (Receiver) share a common clock with each other, or the transmitter provide a clock frequency signal so that the receiver knows when to "read" the next bit of the data. In many forms of this type shows transmission if there is no data at a given instant to transmit, a blank bit must be sent so that data is always being transmitted.

Asynchronous Serial Transmission: Asynchronous serial communication describes asynchronous transmission in which a starts signal is sent to each byte or characters word and a stop bit is sent after each received signals [6]. The start signal prepare the receiving mechanism for the reception of the digital information of a symbol and the stop bit bring the receiving mechanism to rest in preparation for the reception of the next symbol.

III. UART BLOCK

The UART is a serial interface with a frame start bit of active low '0' and 8 bit of information with a stop bit of active high '1'signal at the end. The operation of UART is controlled by the asynchronous clock signal and both the transmission and reception is done respectively with the help of duplex model of UART.

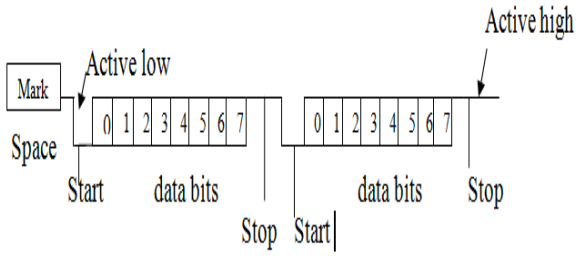

Fig3. UART interfacing with clock signals

The UART mainly consist of three sub modules which help to transfer or receive data with high Speed, accuracy, lower power with higher flexibility.. They will observe the byte or control the data bytes or control words with respect to data received.

UART Receiver: The UART receiver circuit receives a serial input (RX) convert the serial data into parallel one and process the same. It mainly consists of data registers and receivers. The clock frequency is sixteen times than Transmitter with the help of baud rate of the serial data transmission It can easily produces an eight bit parallel output (Data_Rx (7:0)) and provides a status output (DR) that becomes logic 1 when a byte of data has been received. The implementation of UART Receiver can be done using HDL in Xilinx software and shown in figure given below. Considered here:

1. One start bit (logic 0)
2. Eight data bits are transmitted (LSB first, MSB last)
3. One stop bit (logic 1)
4. No parity checking.

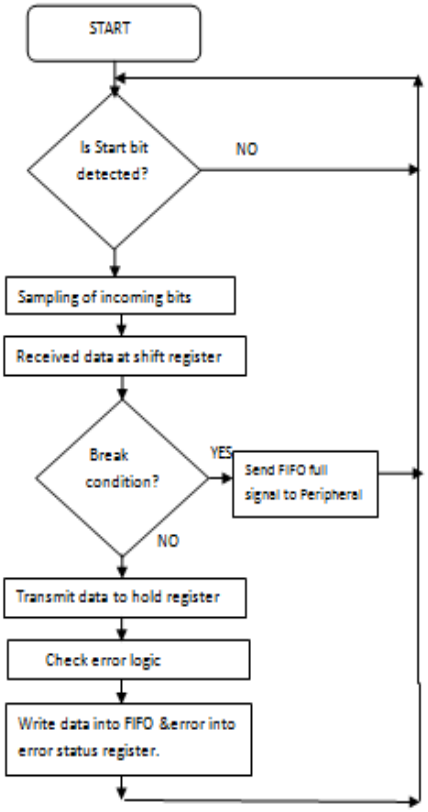

Fig4. Flow Chart of UART Receiver

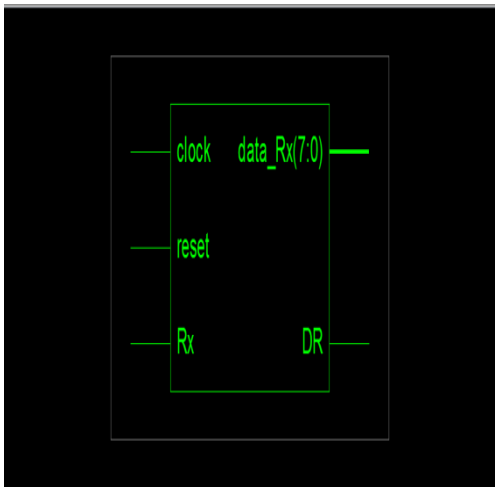

Fig.5 Testing view of Receiver (RTL)

In designing of digital circuit, (RTL) design is used in (HDL) like verilog and VHDL to create high- level representation of a circuits and also visualize the logic gates, multiplexers, encoders, decoders etc in the register transfer logic design. From which low level

representation and ultimately actual wiring can be derived..

UART Transmitter: UART Transmitter: - Transmission operation is easier since it is under the control of the transmitting system. As the data is transferred to shift register after completing of the previous one, the UART generates a frame containing start bit, stop bit, shifts the required the number of data bit out to the line, generates the parity bit if needed and also generate the frame of the Transmission section and show the stop bits and hence the data can be transmitted [9].

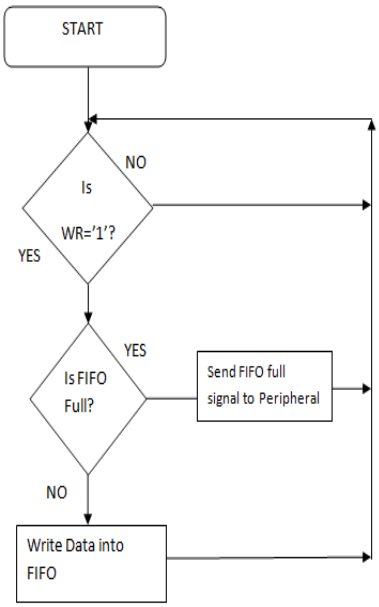

Fig.6 Flow Diagram of UART Transmitter

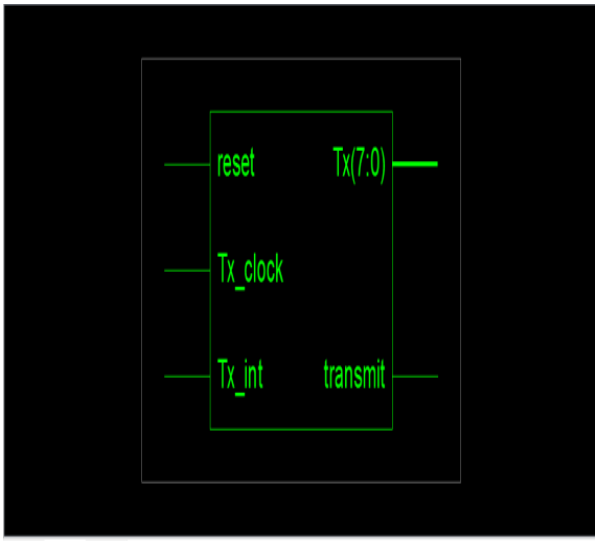

Fig7.Testing view of transmitters (RTL)

UART Baud rate generator: The baud unit is named after Emile Baudot, the inventor of the Baudot code for telegraphy, and is represented in accordance with the rules for SI units. Baud rate generator is nothing but the frequency divider (signal change per second). In UART we will apply the synchronized clock signal to the both receiver and transmitter. The clock signal applied to the receiver is 16 times than the Tx [7]. The baud rate generator generates a sampling signal whose frequency is exactly 16 times UART's baud rate.

Table I. Baud Rate Selector Table

Select	Baud rate
00	9600
01	4800
10	38400
11	19200

In the above representing table, the baud rate generator has to be select only two bits logic as in table to decide the baud rate for receiver and transmitter.

With the help of baud rate, we can easily command on receiver and transmitter. Higher the value of baud rate the controlling and observability action of the UART receiver and transmitter is much increased. Also the value of scan path technique observed clearly and observes the rates.

IV. SCAN PATH TECNIQUE

Scan path is a technique which is used to increase the controllability and observability of logic combinational circuits using scan register into the circuit design [8]. These registers are normally act as a flip- flop but we can switch them into the test mode where they all become a long shift register this help us to Make the data to be clocked serially and pass through all scan registers and get a output through output pin as the same time new data is clocked as input to it.

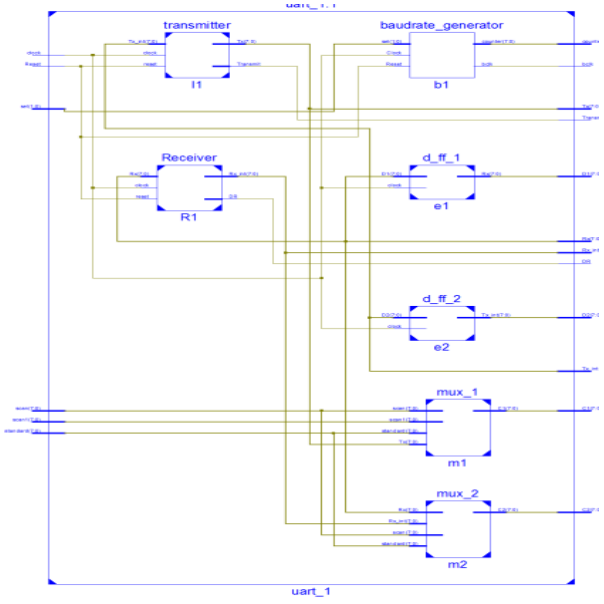

Fig.8 RTL view of Scan Path Technique

Steps1: Set the mode to test and let latches accept data from scan-in input.

Step2: Verify the scan path.

Step3: Scan in the desired state vector into shift register

Step4: Apply the test pattern to primary input pins.

Step5: Set the mode the normal and observe the primary output of the circuit after sufficient time for propagations.

Step6: Assert the circuit clock for one machine cycle.

Step7: Repeat steps 3-6.

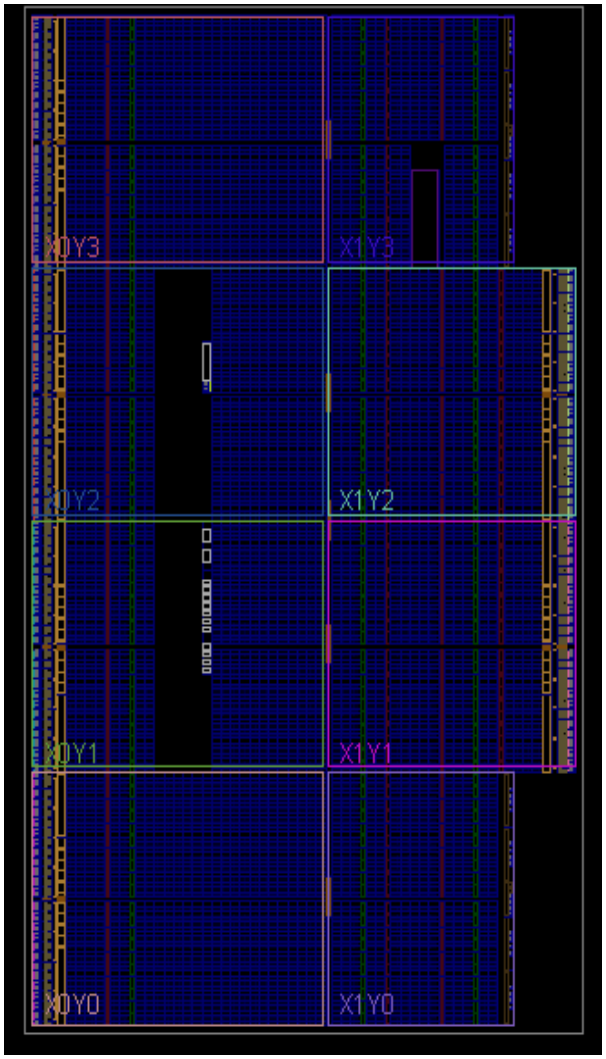

Fig.9 UART using (SPT) On FPGA kit Implementation

V. RESULT AND SYNTHESIS

Register-transfer level (RTL): It shows the blue print image of a design in which the modeling of universal asynchronous receiver and transmitter digital circuits is done through the combinational use of logic gates, multiplexer, encoder, decoder, and various other flows of digital circuits and signals between hardware registers [9].

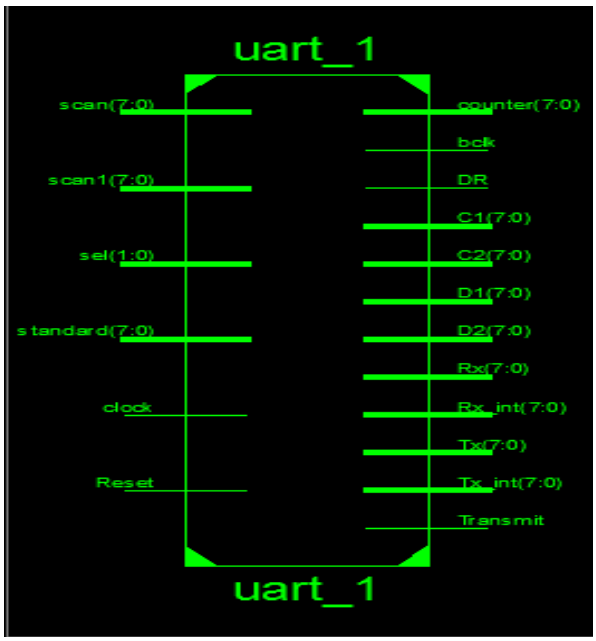

Fig.10 RTL of the system

Fig11. Register transfer level

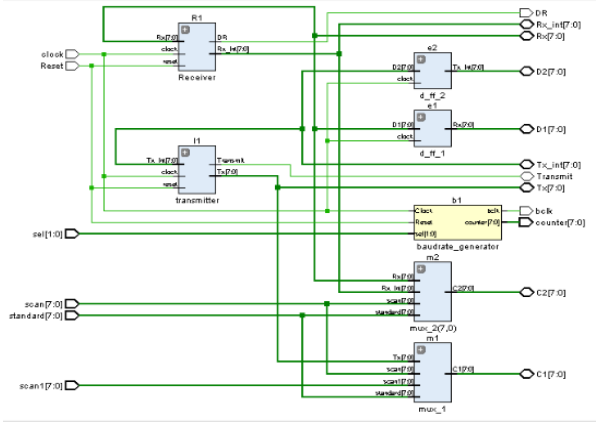

Fig.12 In-between UART chip

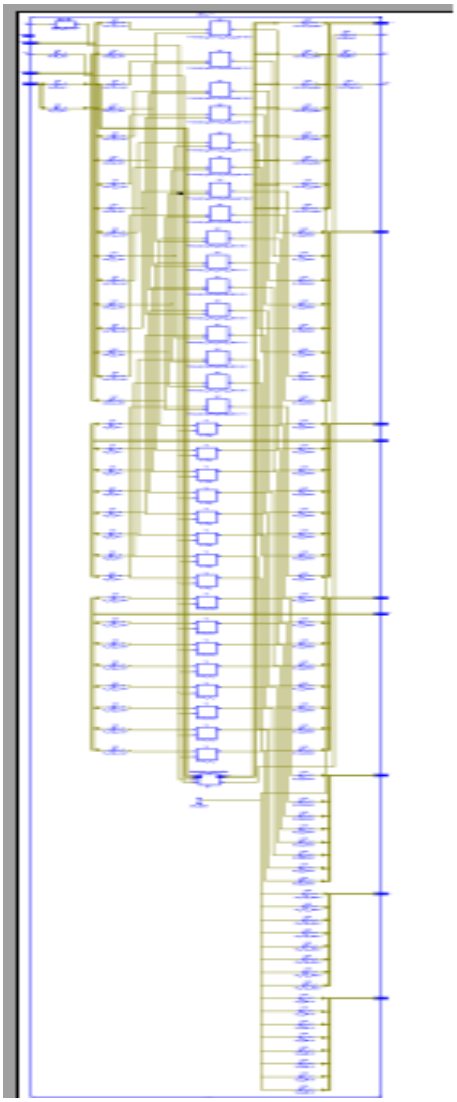

Fig13.Technology Diagarm

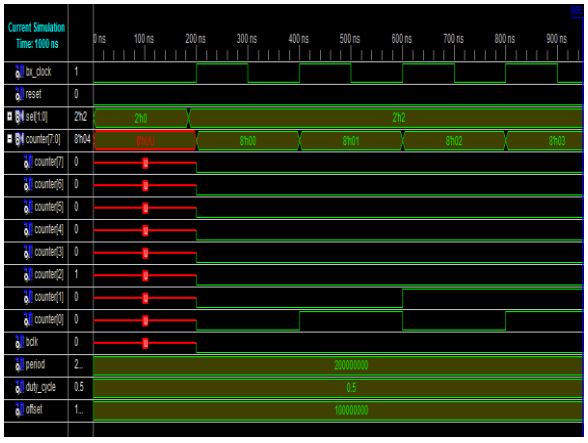

Fig14.Testench Waveform

Simulation: The verification of above design has been done through Xilinx v10.1 1and the test bench waveform has been done through Xilinx software v 10.1. Realization of output waveform has been done through various gates, logic gates, LUTs are shown in above figure.

VI. CONCLUSION & FUTURE SCOPE

The novel design developed in this article is appropriate according to modern technology. We have design Dynamic UART with using Scan Path Technique which is operating fine and can be customized to make it free from over run error. A survey of various methods for implementation through serial communication has been done but the scan path technique provides the controllability and observability and hence we can defined and use the previous bits without recalling again in the loop while the transmission and reception has been done.

Table II. Comparison Between Old Research And Proposed UART

S.N.	Parameter	Virtex4vfx 12sf363-10 [10]	Virtex4fvx 12sf363-10	Scan Path Technique (Dynamic UART)
1.	Numbers of slices	63	36	14
2.	LUT's	109	90	22
3.	GCLK	2	1	1
4.	Slices of flip flop	63	46	19
5.	Maximum frequency	286.151 MHz	284.075 MHz	151.446 MHz
6.	complexity	High	High	Low
7.	size	Large	Large	Medium
8.	FSM	Yes	Yes	No

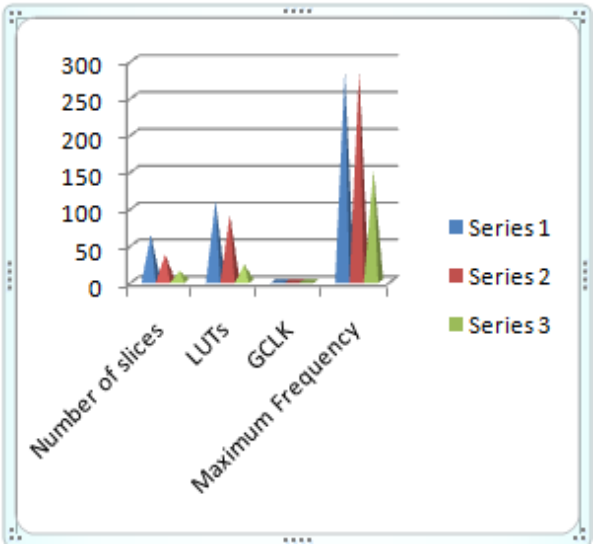

Fig15. Statistical representation

In the above statistical representation of the different parameter Shown in series 1, 2, and 3 like [1]Number of slices, [2]LUT's, [3]GCLK, and [4]Maximum frequency. This design is operated at the maximum Frequency of 151.446 MHz and using only 22 LUT's Blocks as compared to 109 and 90. Where in percentage it uses only 9% of LUT's as compared to 49% and 42% of LUT's are used by others.

VII. REFRENCES

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