A Boost Converter with Ripple Current Cancellation Based On Duty Cycle Selection

Jessin Mariya Jose¹, Saju N²

¹P G Scholar, Electrical & Electronics Engg., NSS College of Engineering, Palakkad, Kerala, India
²Associate Professor, Electrical and Electronics Engg., NSS College of Engineering, Palakkad, Kerala, India

¹jessinjs@gmail.com, ²sajunsspkd@gmail.com

Abstract: In this paper a boost dc-dc converter is proposed based on the concept of ripple current cancellation. This proposed system has the capability of cancelling the input current ripple at an arbitrarily preselected duty cycle. This is accomplished without increasing the count of the number of components in contrast to other solutions available in the conventional system. In addition to this, the converter also features a high voltage gain without utilizing extreme values of duty cycle or boosting transformers. These features make the converter ideal to process electric power coming from low-voltage power-generating sources, such as renewables. This system also provides details on the principle of operation via topological considerations and a mathematical model. The key factor of reactive component sizing is also discussed in detail. The proposed boost dc-dc converter is evaluated by simulating in MATLAB/Simulink software.

Keywords: Boost converter, Complete charge interchange (CCI), Current ripple cancellation, Duty Cycle Selection, Switched capacitor (SC)

1. INTRODUCTION

DC–DC converters are widely used in today’s industrial or commercial electronic devices to manipulate a dc voltage source. As the name states, dc – dc converters work exclusively to take a dc voltage input and convert it to output at a different level of dc voltage. They can either step-up or step-down the input dc voltage while maintaining minimal power loss during the process. There are many different topologies available for use such as Buck (step down), Boost (Step up), Fly back, Push-Pull, etc.

Owing to worldwide energy crisis and awareness of environmental protection in recent years, a substitute for energy has become an important issue. Among many substitute energies, solar energy, wind energy, hydroelectric power, biomass energy, and fuel cells are common and these are green energies with potential development.

A fuel Cell is a device that converts the chemical energy from a fuel into electricity through a chemical reaction with oxygen or another oxidizing agent. The fuel cell is one of the most promising power supplies and is drawing attention by many researchers. Due to high efficiency, high stability, low energy consumed and friendly to environment, this technology is in the progress to commercialize.

The voltage provided by a number of small power generating sources such as renewable is usually low in amplitude. As a result of this, a boost-type architecture with a large voltage gain is required to link this voltage to an inverter.

One of the major challenges in designing these type boost especially for high power applications is how to handle input current at both input and output. Another important requirement for a converter in renewable energy applications (for example, in fuel cells) is to drain a continuous current with minimum ripple. Therefore, converters combining these two features are expected to find many applications within the renewable-energy context. A traditional boost converter can achieve an infinite voltage gain as the duty cycle approaches 100% in theory, but in practice, the leakage resistance in the inductor-charging loop limits the boost ratio [1], [2]. Because of this, a boost converter is not used when the required boost ratio is higher than four. An approach to overcome this drawback is by increasing converter’s switching frequency by using small reactive components for a given amount of acceptable ripple.

However, the finite switching time in actual power semiconductors limits the switching frequency when the duty ratio is too small or too high. A traditional solution to this is the employment of intermediate transformers to increase the voltage without using extreme values of duty cycles.

Several topologies have been proposed in the literature for overcoming those challenges, including the use of coupled inductor and/or transformers. Compared to basic converter topologies, pwm converters with quadratic dc conversion ratio offer a significantly wider conversion range. M (vo/vin) is a function of duty ratio. But in quadratic converters the numbers of components are more and also there is voltage stress across switches [3]. Quadratic converters can somehow alleviate the efficiency problem of cascade circuits using a single driven transistor. But they may present voltage or current over stress [4]. Converters with the coupled inductor in the second boost converter can effectively extend the voltage conversion ratio and the it also benefits the input ripple cancellation [5]. A dual inductor boost converter is applicable for high voltage gain applications. It has some features as high voltage gain with smaller transformer turn ratio, voltage stress is reduced [6]. By using both coupled inductors and isolated transformer, high voltage gain can be easily achieved without extremely high duty ratio [7].
Another converter that uses the coupled-inductor and switched capacitor techniques can achieve high voltage gain and high efficiency, the capacitors can charge in parallel and discharge in. series by the secondary side of the coupled inductor. However, the leakage inductor of the coupled inductor may cause high power loss and high voltage spike [8]. By integrating full-wave rectifier with a classic current-fed converter as an example, a dual-inductor boost converter with ripple cancellation is presented. It has several features, such as high voltage gain with smaller transformer turns ratio, recovery of the transformer secondary leakage energy, low voltage stress on the rectifier diodes, and non-pulsating input and output currents. These properties make it desirable for high-frequency high efficiency high-voltage-gain applications, such as the renewable energy source power system. [9]. The converter achieves high step-up voltage gain with appropriate duty ratio and low voltage stress on the power switch. A new high step-up DC-DC converter designed especially for regulating the DC interface between various micro sources and a DC-AC inverter to electricity grid. [10].

Another main challenge in a renewable-energy power processing circuit is the expected low input current ripple. The Standard solution of using large inductors leads to a small current ripple, but large inductors are heavy, large in size, and expensive. In addition, a large inductor also slows down transient response of the converter. The topology proposed in this paper corresponds to an improved and different version of an approach recently proposed in the literature [11].

Herein, a new dc-dc boost converter topology is proposed which combines two principles: 1) At the converter’s input, two inductors are interleaved for cancelling the input current ripple, and 2) at the converter’s output, an SC voltage multiplier is utilized to increase the voltage gain. By using a small resonant inductor the AC stage has been improved in order to limit the peak current resulting from the switching process and hence preventing large current spikes. The new proposed topology herein is able to cancel the input current ripple. Furthermore, it combines a CCI-SC circuit with a boost converter into a single converter and is able to provide voltage regulation without sacrificing the converter’s efficiency.

II. PROPOSED TOPOLOGY

The improved boost converter topology is shown in Figure 1 As the figure suggests, the topology contains two transistors (S1 and S2), three diodes (d1, d2, and d3), three capacitors (C1, C2, and C3), two inductors for energy storage (L1 and L2), and a small inductor (L3) for current limiting through d3. In practical implementation, L3 is around 100 times smaller than L2 and 50 times smaller than L1. As a result of its reduced size, small-ripple approximations do not apply to L3, and hence, the selection of its inductance is based on the CCI between C2 and C3.

![Fig 2.1 Circuit of the new topology](image)

The transistors switch complementarily, i.e., when S1 is closed, S2 is open and vice versa. The operation of the converter may be explained considering the small-ripple approximation for the voltage across capacitors and continuous conduction mode for L1 and L2. The details on the circuit operation are conveniently introduced by employing several analytical waveforms. As shown in Figure 3.2 and 3.3, the converter has two equivalent circuits resulting from the switch action. When S1 is on (and S2 is off), the topology is represented by the equivalent circuit in Figure 3.2. During this time, the diode d1 is reversed biased, blocking the voltage across C1. Similarly, diode d3 is reversely biased, blocking the voltage across C3. The current through L2 forces the diode d2 to be closed since transistor S2 is open.

![Fig 2.2 Equivalent circuit when S1 is on](image)
Fig. 2.3 Equivalent circuit when S2 is on

The typical waveforms for the currents through L1 and L2, the input current, and the switching sequence for S1 and S2 are shown in Figure 3.4 from top to bottom. While S1 is conducting, the current through L1 rises with a slope of \( \nu_1 L_1 \), and L2 discharges at a rate of \( \nu_2 L_2 \).

On the other hand, while S2 is on (and S1 is off), the resulting equivalent circuit is as shown in Figure 3.3. During this time, the L1 discharges with a slope that is equal to \( \nu_1 L_1 \), while L2 charges at a rate of \( \nu_2 L_2 \). Furthermore, while S2 is conducting, the capacitors C2 and C3 are connected in parallel, leading to an SC-type behavior. As a result of this, a small inductor (L3) is needed in order to limit the peak current around this loop. A typical waveform for the current through L3 is also shown in Figure 3.4. A key feature of the boost converter topology is as shown in Figure 3.3. The current waveforms shown in Figure 3.4 correspond to a converter that features a zero input current ripple at a duty cycle of \( D = 75\% \). This is possible if both inductors are charged with the same voltage and \( L_2 = 3L_1 \).

III. PRINCIPLE OF SWITCHED CAPACITOR

A switched capacitor is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously.

The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S1 and S2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge q from the input to the output at the switching frequency f.

IV. VOLTAGE ANALYSIS

The dynamics of L1, L2, and C1 may be conveniently analyzed considering their average behaviour, as their state variables feature triangular waveforms similar to those in traditional dc/dc converters. On the other hand, C2, C3, and L3 form a SC circuit, and therefore, their dynamic behaviour has to be formulated with additional considerations. However, a number of the converter's features can be explained focusing on L1, L2, and C1, where dynamic averaging applies. Under this assumption, switching functions may be readily replaced by their corresponding duty cycles. For the analysis hereinafter, the converter's duty ratio \( d(t) \) is defined as percentage of time over the switching period that the switch S2 is on, i.e.,

\[
d(t) = \frac{1}{T_S} \int_{t}^{T_S} q_2(T) dT
\]  

(1)

Where TS is the switching period and q2 is the switching function of s2 that is equal one while s2 is closed and zero otherwise. Under this assumption, and neglecting inductors’ for now equivalent series resistance (ESR), the equations that represent the average dynamics for inductors L1 and L2 are

\[
L_1 \frac{d_1}{dt} = d_1(v_{in} - v_{C1}) + (1 - d_1)(v_{in})
\]  

(2)

\[
L_2 \frac{d_2}{dt} = d_2(v_{in}) + (1 - d_2)(v_{in} - v_{C2})
\]  

(3)

In steady state, the average voltage across the inductors must be equal to zero. Thus, by zeroing the left-hand side of (2) and (3), the steady state voltage across C1 and C2 may be expressed as

\[
V_{C1} = \frac{1}{D} V_{in}
\]  

(4)

\[
V_{C2} = \frac{1}{(1-D)} V_{in}
\]  

(5)

In (4) and (5) (and through the rest of this paper), capital letters denote steady-state quantities. It readily follows from (4) and (5) that the voltages across C1 and C2 are proportional to one another, i.e.,

\[
V_{C1} = \frac{(1-D)}{D} V_{C2}
\]  

(6)

\[
V_{C2} = \frac{D}{(1-D)} V_{C1}
\]  

(7)

On the other hand, the equation that represents the average dynamics for C1 is
In steady state, the average current through C1 must be equal to zero, which leads to the following expressions for the current through L1:

\[ I_{L1} = \frac{1}{D} \left( \frac{V_{C1} + V_{C3}}{R} \right) \]  

As C2 and C3 form an SC circuit, average dynamic equations do not apply. However, the steady-state current through L2 can be computed by input/output power balance considerations. It becomes

\[ I_{L2} = \frac{1}{(1-D)} \left( \frac{V_{C1} + V_{C3}}{R} \right) \]  

Furthermore, from Fig. 2.1, the output voltage is

\[ V_O = V_{C1} + V_{C3} \]  

Thus, combining (4), (5), and (9)–(11), the converter gain becomes

\[ \frac{V_O}{V_{in}} = \frac{1}{D(1-D)} \]  

As mentioned earlier, this circuit has an SC stage which may be increased by including additional capacitors and diodes [1]. Capacitors C2 and C3 work in an SC way because C2 clamps the voltage across C3 while the switch s2 is closed. This is because the energy stored in L3 is negligible compared to other energy storage elements in the converter. Furthermore, in steady state, C2 and C3 feature the same average voltage.

\[ V_{C2} = V_{C3} \]

The gain expressed by (12) corresponds to an ideal case as the inductors’ ESR has been neglected.

By construction, a smaller inductor features a smaller ESR. As explained earlier, the topology proposed herein sizes the inductors to cancel the input current ripple at a given duty ratio. For example, if \( L_2 = 3L_1 \), the input current is ripple free at \( D = 75\% \). As a first approximation, it may be assumed that the inductor’s ESRs follow the same trend, i.e., \( RL_2 = 3RL_1 \). Fig. 2 shows the converter’s voltage gain under this assumption for different values of the ratio between the load resistance (R) and RL2. The figure is readily obtained by plotting.

As the figure suggests, the minimum voltage gain is four and occurs at \( D = 50\% \). If the duty cycle is smaller than 50%, the gain increases again, and therefore, the minimum gain that the converter can operate is around four. The operating range is selected to be at \( D > 50\% \), which ensures that L3 will have enough time to discharge.

As a result, the selection of the inductors has to be such that \( L_2 > L_1 \), in order to achieve ripple cancellation for the input current. Furthermore, \( L_2 > L_1 \) implies that \( RL_2 > RL_1 \), and thus, larger voltage gains are obtained for \( D < 10\% \), which can be observed in Fig. 2. This is a compromise between cancelling the input current ripple and obtaining a larger voltage gain. However, in practical applications, dc/dc converters are operated at duty cycles of about \( 20\% < D < 80\% \). It can be seen from the figure that, between that range, the voltage gain is practically symmetric, and hence, the voltage gain lost is minimal. It is noteworthy that selecting \( D > 50\% \) as the operating range translates into having the SC part of the converter handling a larger amount of the converter’s throughput power. The figure also suggests that, as in most dc/dc converter’s topologies, the inductor’s ESR limits the practical gain of the approach. Therefore, this topology is more suitable if a large switching frequency is employed as, in that case, reactive components (and, hence, ESRs) are very small.

V. SIMULINK MODEL AND RESULTS

The converter proposed herein was simulated in MATLAB/Simulink software in order to validate its principle of operation. The simulation circuit is as shown by the Figure 5.1. The list of parameters i.e. values of each component in the circuit is shown in the TABLE 5.1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT VOLTAGE</td>
<td>15 V</td>
</tr>
<tr>
<td>DUTY CYCLE</td>
<td>70 %</td>
</tr>
<tr>
<td>OUTPUT VOLTAGE</td>
<td>71 V</td>
</tr>
<tr>
<td>( L_2 )</td>
<td>140 ( \mu )H</td>
</tr>
<tr>
<td>( L_4 )</td>
<td>330 ( \mu )H</td>
</tr>
<tr>
<td>( L_5 )</td>
<td>28 ( \mu )H</td>
</tr>
<tr>
<td>( C_1, C_2, C_3 )</td>
<td>10 ( \mu )F</td>
</tr>
<tr>
<td>SWITCHING FREQUENCY ( F_s )</td>
<td>25 kHz</td>
</tr>
</tbody>
</table>

A. Simulink Model

![Fig 5.1 Simulation Model](image-url)
B. Simulation Results

Fig 5.2 Waveform of Input Voltage

It is evident from the simulation results that the input current is almost ripple free. A closer examination of the measurements also suggests the simulation data's are consistent with the values obtained as per the design.

VI. CONCLUSIONS

This paper has presented a boost dc–dc converter topology, with the novel capability of cancelling the input current ripple at an arbitrarily preselected duty cycle. This is accomplished without increasing the count of the number of components. In addition, the converter features a high voltage gain without utilizing extreme values of duty cycle or boosting transformers. These features make the converter ideal to process electric power coming from low-voltage power-generating sources, such as renewable. The boost factor or voltage gain may be extended by utilizing diode-capacitor multipliers. Those features are highly desirable in fuel cell applications

Moreover, the rapid development of silicon carbide and other wide-band gap fast-switching power semiconductors will enable the use of smaller reactive components and hence provide further advantages to the approach presented herein against transformer or coupled-inductor-based topologies. Simulation results are consistent with the analytical predictions of the various formulas developed through this paper, and hence, the approach may be considered definitely validated.

ACKNOWLEDGMENT

All glory and honour be to the Almighty God, who showered His abundant grace on me to make this project a success. I would like to express my deep sense of gratitude towards Prof. Sapna Gopal (Head of the Department, Dept. of Electrical and Electronics Engineering) for providing all the facilities for making my project a successful one. I extend my Sincere thanks to Prof. Saju N (Associate Professor, Dept. of EEE), for his guidance and support. I also convey my sincere thanks to the M-Tech Coordinator Dr. E. G Janardhananand members of staff for wholehearted co-operation in completing the project.

I express my sincere gratitude to all the members of staff who helped me with their timely suggestions and support. I also express my sincere thanks to all my friends who helped in all the conditions.

VII. REFERENCES


