

Analysis and Implementation of H-Bridge Inverter for Minimizing THD

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Abstract: This paper projects the different levels of cascaded H-bridge inverters and the minimization of total harmonic distortion by increasing the levels. For triggering of the semiconductor devices used in the inverter level shifting pulse width modulation technique is used. Individually for each level inverter we have developed the switching circuit and also the inverter. The analysis of three level and five level cascaded H-bridge inverters is done in MATLAB/SIMULINK by applying level shifting PWM technique. The simulation results shows the improvement of output voltage waveform and reduction of the total harmonic distortion by increasing the levels in inverter.

Keywords: Cascaded H-bridge inverter, Level Shifting, Pulse Width Modulation.

I. INTRODUCTION

The Voltage source inverter fed induction motor drives are mostly used in medium power applications. The voltage waveforms of two level inverter show that the voltage across the motor contains not only the required fundamental sinusoidal components, but also pulses of voltage i.e. ripple voltage. The output of inverter voltage is applied to the induction motor then the performance of the motors are degraded. Because of the ripple voltages the rate of change of voltage with respect to time is more. Also high voltage rating of the power semiconductor devices is required for inverters used to run the high voltage motors. The medium and high voltage induction motor drives required high level inverter to produce the waveforms nearer to sinusoidal and to minimize the ripple content. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors. The three and five level cascaded H-bridge inverters are analyzed how to produce the sinusoidal voltage and how the switches are operated with the level shifting PWM.

This paper is organized into five sections. Following the introduction in section I, different levels of inverters are

discussed in section II, the basics of the level shifting PWM in section III, the simulation of three, five and seven level inverters with results and comparison between them in section IV. Finally conclusion from section V.

II. CASCADED H-BRIDGE INVERTER

The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, like batteries, fuel cells, solar cells, and ultra-capacitors. A single-phase structure of a cascade inverter with separate dc sources [1]. Each separate dc source is connected to a single-phase full-bridge inverter. Single phase topology of the hybrid multilevel inverter is shown in Fig.1; the bottom is one leg of a standard 3-leg inverter with a dc power source V_{dc} , the top is a hybrid in series with each standard inverter leg that the H-bridge inverter can use a separate dc power source the top is a hybrid in series with each standard inverter leg that the H-bridge inverter can use a separate dc power source ($V_{dc}/2$).

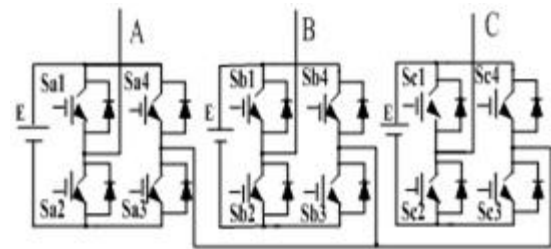


Fig.3 Three Level Cascaded H-Bridge Inverter

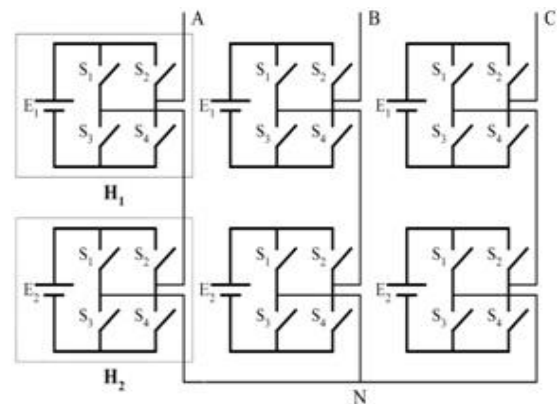


Fig.4 Five Level Cascaded H-Bridge Inverter

Considering the output voltage V_1 of this leg is either $+(V_{dc}/2)$ when S_1 is closed or $-(V_{dc}/2)$ when S_2 is closed. This leg is connected in series with a full H-bridge inverter, then the output voltage V_2 of the H-bridge inverter is either $+(V_{dc}/2)$ when S_{a1} and S_{a4} are closed, 0 when S_{a1} , S_{a3} or S_{a2} , S_{a4} are closed, or $-(V_{dc}/2)$ when S_{a2} and S_{a3} are closed. An example output waveform that this topology can achieve as shown in the Fig. 2. The topology of the proposed a 5-level 3-phase cascaded hybrid multilevel inverter is shown in Fig. 3.

III. SWITCHING PATTERN SCHEME

In this paper, a level shifted pulse width modulation technique is employed.

A. Level Shifted PWM

An m-level Cascaded H-bridge inverter using level shifted modulation requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. The frequency modulation index is given by. Level shifted PWM technique is classified into three types. 1) In phase disposition 2) Phase opposition disposition 3) Alternate phase opposition disposition.

1) *In Phase Disposition*: In phase disposition method all the carrier waves are in phase with each other as shown in figure below

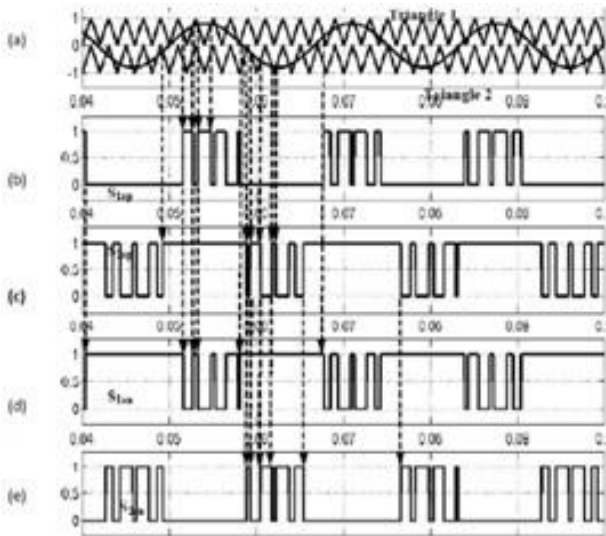


Fig.6 Switching Pattern in IPD

2) *Phase Opposition Disposition*: In phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero as shown in figure below

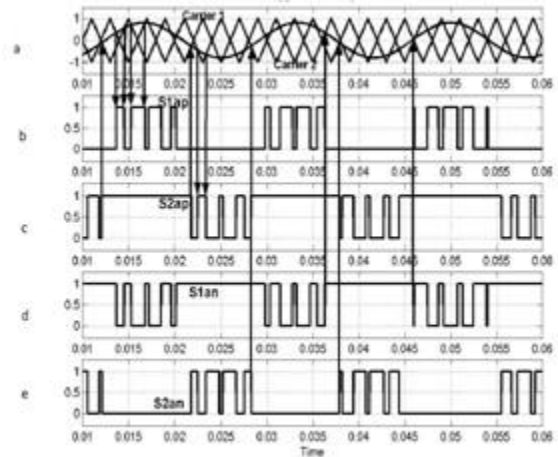


Fig.7. Switching Pattern in POD

3) *Alternate Phase Opposition Disposition*: In case of alternate phase disposition modulation, every carrier waveform is in out of phase with its neighbor carrier by 180° as shown in figure below.

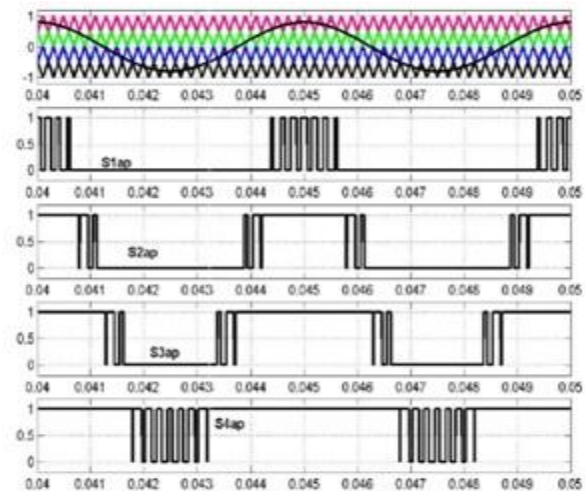


Fig.. Switching Pattern in APOD

IV. MATLAB MODELING AND SIMULATION RESULTS

In this simulation is carried out in following three cases.

- i) Cascaded 3-level inverter with pulse width modulation.
- ii) Cascaded 5-level inverter with pulse width modulation.

Case i: In this case we will find out output voltage and Total Harmonics Distortion for 3-level cascaded H-bridge inverter. The simulation diagram and corresponding waves forms are as shown in figure.

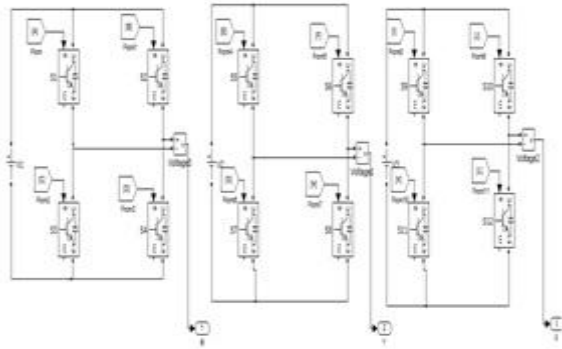


Fig.9 Three-Level inverter

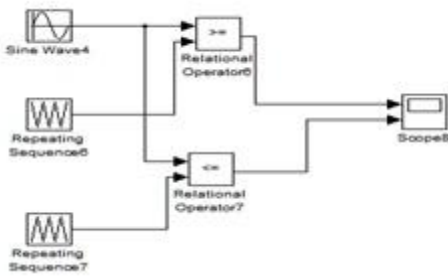


Fig.10 Switching Circuit

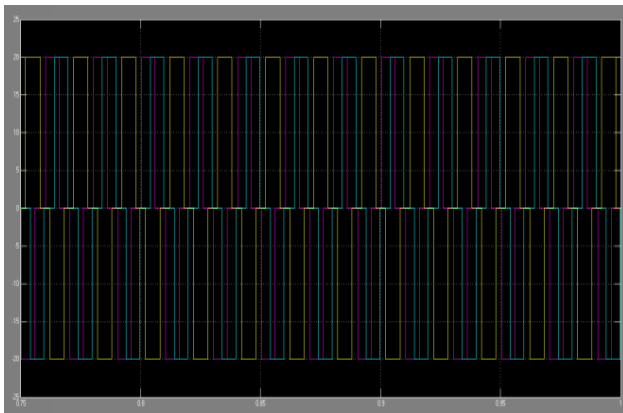


Fig.11 Line Voltage Of Cascaded 3-Level Inverter

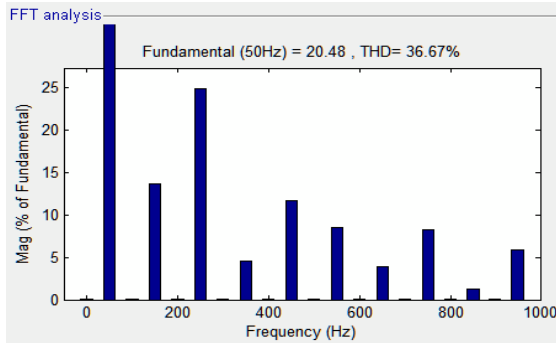


Fig.12 THD Analysis of 3-Level Inverter With Level Shifted PWM.

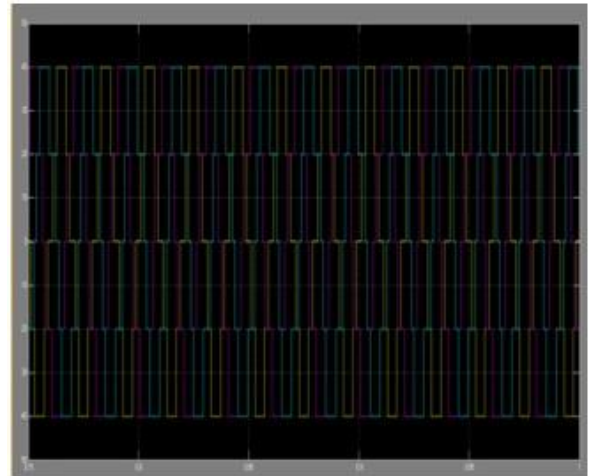


Fig.13 Line voltage of 5-level cascaded H-bridge inverter.

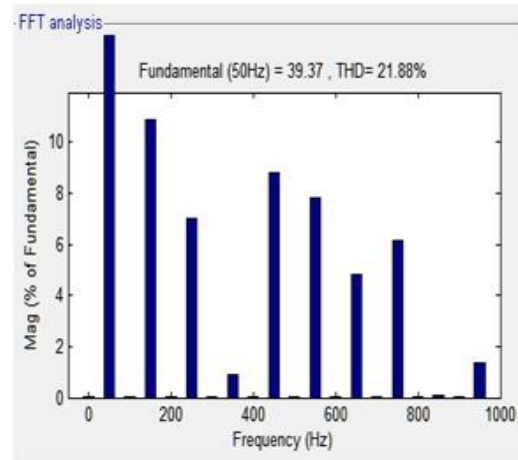


Fig.13 THD Analysis of 5-Level Cascaded H-Bridge Inverter.

Table

| Levels | % TDH |
|--------|-------|
| 3 | 9.88 |
| 5 | 2.78 |

V. CONCLUSION

In this paper a three level and Five level cascaded H-bridge inverter with level shifted PWM has been designed and compared their THDs. From the comparison we have to identify as level of the inverter is increases the Total Harmonics Distortion and the machine performance is improved.

VI. REFERENCES

- [1]. Keith Corzine and Yaakov Familiant "A New Cascaded Multilevel H-Bridge Drive."IEEE

Transaction on Power Electronics, Vol.17, No.1,
January2002.

- [2]. Rodriguez, J.S. Lai, Fang Z. Peng, (2002) "Multilevel Inverters: A Controls and Applications", Survey of IEEE Trans Topologies, on Industrial Electronics, Vol 49, No 4, 724-738.
- [3]. T.Prathiba*, P.Renuga,(2012) "A comparative study of Total Harmonic Distortion in Multilevel inverter topologies",JIEA,Vol 2,No 3.
- [4]. Zhong Du, LeonM.Tolbert, BurakOzpineci, John N. Chiasson, (2009) "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter" IEEE transactions on power electronics, vol. 24, no. 1.
- [5]. Leon M. Tolbert, T.G. Habetler, (1998) "Novel LEVELS %THD Multilevel inverter Carrier-Based PWM Methods", IEEE IAS Annual meeting, Oct. 10-15, 1424-1431.
- [6]. N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in Proc. IEEE PESC'91,1991,pp.96–103.