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A Review on Various Techniques to Design 2/3 Prescaler

Jasbir Kaur[1], Mohit Sharma[2]
[1]Jasbir Kaur, Assistant Professor, ECE Dept., Punjab Engineering College, Chandigarh
[2]PG Scholar, VLSI Design, PEC University of Technology, Chandigarh
[1]jasbirkaur.co.pec.in, [2]mohit8293@gmail.com

Abstract: A lot of variations are seen in present circuits because of intensive scaling. In this paper various 2/3 prescalers and their working operation has been discussed. This work compares various known 2/3 prescalers circuits and then identifies the circuit on the basis of speed and power taken into consideration. Throughout this paper the total power consumed by this circuit and the maximum operating frequency of various 2/3 prescalers circuits are discussed. ETSPC (Extended True Single Phase Clock) turned out to be the most efficient in terms of speed when compared with other circuits. The 2/3 prescaler with minimum delay and power is reported, to help the designer in selecting the right fit design depending on their specific requirements.

Keywords: TSPC, ETSPC, Switching Power, Short Circuit Power, DFF(D Flip Flop).

I. INTRODUCTION

A 2/3 prescaler is the most widely used prescaler due to its high speed as compared to other prescalers. These are made up of flip flops which are almost a significant component of every sequential circuitry. Among various prescalers, 2/3 prescaler is commonly used. Current Mode Logic(CML) latch is used in conventional flip flop based dividers, but disadvantage of large load capacitance is present. Due to this maximum operating frequency is reduced and total power consumption is increased. Flip flop based frequency divider uses dynamic logic flip flops like TSPC(True Single Phase Clock) and this design can be improved by using ETSPC(Extended True Single Phase Clock) flip flops for more Speed in less power application. A 2/3 prescalar divided the input frequency of the clock by 2 or by 3 depending upon the mode in which it is working, as it does work in duel mode. If the timing delay is taken into consideration due to large number of flip flops used in frequency dividers made by cascading 2/3 prescalers is considerably large which consequently increases the operating frequency.

In the past few decades CMOS technology have gone through drastic scaling with the view of circuit density, high speed and low power dissipation. Presently, some more hurdles have come into picture, which are more critical than earlier.

Delay and power are the most considerable parameter in designing the circuit. There is always a trade-off occurs between these two design parameter, Designing a circuit of given specifications is extremely difficult. These two parameters depend upon the design of the circuit and different type of flip flops used for making 2/3 prescaler.

Keeping in mind the above mentioned problems, this paper investigates for design techniques, delay and power of various 2/3 prescalars. Selection of D flip flop for making 2/3 prescaler is the most crucial step and deciding factor for maximum operating frequency and delay of the circuit. In today's scenario there is a necessity for fast circuits. This makes the selection of the basic circuit elements and prescalers to be the most important part for getting the desired characteristics for the large circuits like frequency divider which is used in PLL.

Keeping this in mind following sections are discussed in this paper:

1) Four different 2/3 dual modulus prescalers circuit are observed.

2) Circuits are analyzed to see the impact of modification in the conventional circuit.

3) Finally the best 2/3 prescaler is concluded in terms of highest operating frequency and delay.

Arrangement of rest of the paper is in this manner. Section II discusses all the four 2/3 prescaler used for comparison. Section III ends up with the conclusion.

II. 2/3 PRESCALER TECHNIQUES

This section briefly describes various 2/3 topologies considered for analysis in this work.

A. Using Pass Transistor Logic Circuit Low Voltage and Low Power Divide-By-2/3 Counter Design Technique.

In figure 1 ETSPC based 2/3 prescaler is shown. In this working frequency is increased by reducing the critical path between the DFFs because maximum frequency depends on the critical path delay in two DFFs which is a dominant factor of the two ETSPC based flip flops. Inverters used between flip flops in [1] and [2] create more delay and parasitic capacitance is also increased due to merging of control logic by connecting them into parallel which also increases delay in the circuit. Basic circuit of the proposed design shown in the figure 2. In this circuit 2 DFFs and 1 AND Gate remains the same but change the OR gate used in [1] by a switch. Output of Q' of DFF1 is given to DFF2 after complimenting it

When switch is open output from DFF1 is disconnected from DFF2 and it works as a divide by 2 circuit. When switch is closed it works as a divide by 3 counter as in [1]. ETSPC is not only good for high speed operation

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but also where low voltage operation is needed. Only one P MOS, which is fed by the control signal works as a switch.

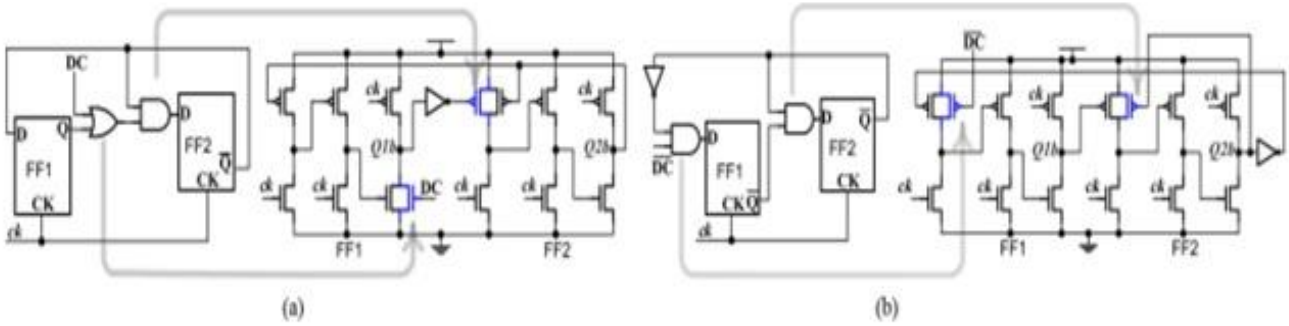

Fig. 1. ETSPC Based 2/3 Design as in (a) [1] (b) [2].

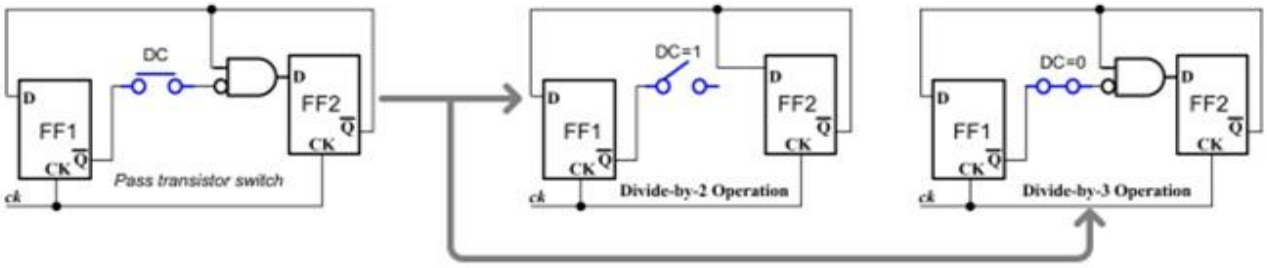

Fig. 2. Logic Circuit of the Proposed Design in [5].

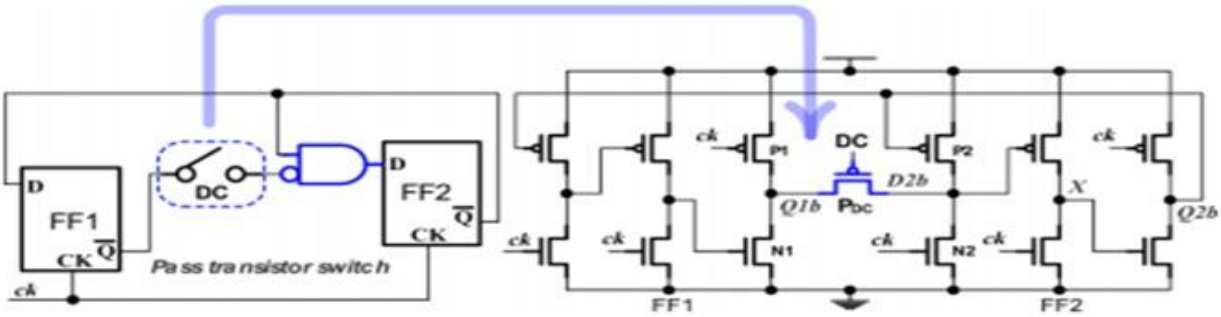

Fig. 3. Proposed Design of ETSPC Based Divide by 2/3 Prescaler Using a Pass Transistor in [5].

Table I. Comparison Between [1], [2] and Proposed Design in [5]

2/3 Counter	Design [1]	Design [2]	Proposed in [5]
No. of Transistor Count	16/4	16/4	13/1
Layout Area(μm^2)	19.51	100.85	71.98
Max. Freq. (MHz) 2/3	475/451	470/470	531/525
Average Power (uW)	6.38/5.92	5.74/5.24	4.35/4.61
Power Delay Product (fJ)	13.43/13.3	12.21/11.15	8.19/8.78

Table I shows the comparison done between the proposed design and the design in [1] and [2]. This is merely not an addition of one pass transistor. Here speed and power characteristics are not changed which makes it better than the designs having logic gates embedded. In addition to that one inverter is also removed which inverts the output of ETSPC to get divide by 3 operation. When DC is low, post flip flops output is given to the first stage output of the second flip flop. When DC is high pDC is off and does not pass the value.

B. ETSPC-Based Prescaler :

Load capacitance is reduced in ETSPC which in turn reduces delay of the ETSPC as compared to TSPC. Maximum frequency at which a TSPC flip flop can be operated is obtained by the f_{max} in [3] by equation (1)

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$$f_{max}=\frac{1}{2\times\max\,(t_{pLH,}t_{pHL,})} \quad (1)$$

Power consumption is also dependent upon maximum frequency. Divide by 2/3 prescaler is used which make less number of components to be used at high speed. The proposed design uses two D flip flops. The circuit operation can be explained in two steps:

1) When the controller signal MC is low it will divide the input frequency by 3. When the output of DFF2 is low, node S1 will be inactive which in turn result in no switching activity at node s2 and s3 and no power will be dissipated. DFF1 works every time while DFF2 works only when DFF2 output goes high.

2) When MC goes high DFF1 output will be inactivated and divide by 2 operation will work. But for the operation of divide by 2 operation only one D flip flop is needed and by the proposed method 50% of the power can be saved. To achieve the reduction in power, a new design of 2/3 prescaler is proposed in [2] to reduce the switching activity in the short circuit activity. Instead of using one OR gate and one AND gate, two AND gates are used as shown in [4], in order to get the symmetry in architecture.

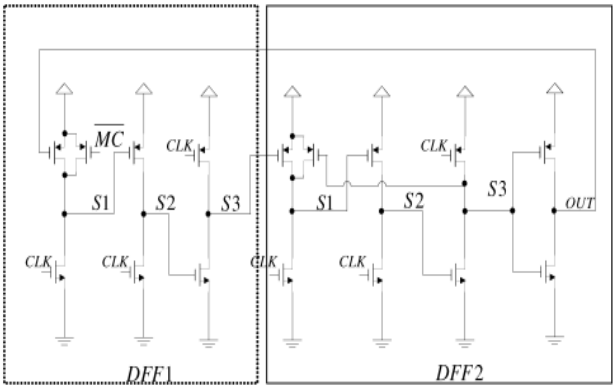

Fig. 4 Proposed Design of ETSPC 2/3 Prescaler [2]

Here MC controlled nMOS is changed to a $\overline{MC}$ controlled pMOS so that DFF1 gets blocked when MC goes high therefore s1, s2, s3 nodes of DFF 1 having values 1,0,1 respectively are jammed. Now DFF has only one short circuit path in the first stage but the remaining stages have no switching activities and short circuits due to which only DFF2 works in divide by 2 operation which reduces power consumption. Even in divide by 3 operation some reduction in power due to decrease in short circuit activity in DFF1 is seen.

For verification purpose an 8/9 dual modular prescaler is made with the same circuit used in [1], but using proposed 2/3 dual modular prescaler as shown in the figure 4. The total power consumption is the sum of two AND Gates and 2 D flip flops, which is due to switching power and the short circuit power. Here in divide by 3 operation a big change in power consumption is not significantly found, however in divide by 2 operation power dissipation has decreased significantly.

$$P_{\frac{2}{3}Pro}=P_{switching-DFF2}+P_{short-DFF2} \quad (2)$$

$$P_{switching-DFF2}=\sum_{i=1}^{4} C_{Li}f_{in}V_{dd}^2 \quad (3)$$

Here C_{Li} is the load capacitance of node s1,s2,s3 and output of DFF2, f_{in} is input frequency,V_{dd} is supply voltage, $P_{switching-DFF2}$ is switching power in DFF2, $P_{short-DFF2}$ is short circuit power in DFF2. From table II it is seen that the reduction in power in proposed method is significantly large as compared to the conventional method.

In divide by two TSPC major power consumption is due to switching activity and this will affect the total power consumption as in divide by 8 operation the majority of the power consumption is due to 2/3 prescaler which is about 50% of the total power consumption as compared to conventional prescaler [1] which accounts for more than 60% of the total power consumption.

Table II. Comparison between Proposed Design and [1].

Design Parameters	Work in [1]	Work in [1] Resimulated	Work In [2] (Sim/measured)
Process (µm CMOS)	0.25	0.18	0.18
Supply Voltage (V)	2.5	1.8	1.8
Max. Frequency (GHz)	2.8	4.5/4	4.5/4
Power (mW)	3.05	3.1/2.9	2.5/3.3

C. TSPC Based 2/3 Prescaler [6]:

Conventional design [6] had two D flip flops, AND gate and one OR gate. As there is large load at DFF2, operation speed is restricted and large power is dissipated. OR gate and AND gate introduces extra delay which decreases the speed. Switching power in the conventional design is given by (4)

$$P_{switching}=\sum_{i=1}^{12} C_{Li}f_{in}V_{dd}^2 \quad (4)$$

Here $P_{switching}$ is switching power, , f_{in} is input frequency, V_{dd} is supply voltage, C_{Li} is the load capacitance of node s1,s2,s3 and output of DFF1,DFF2 and gates. In figure 5 improved design is shown.

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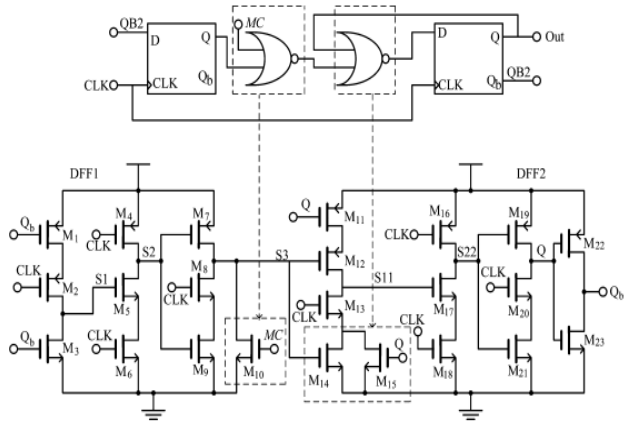

Fig. 5. Proposed Design 1 of TSPC 2/3 Prescaler [6]

In the 3rd stage of DFF 1 using one nMOS transistor first NOR gate is rooted and another NOR gate is embedded to the input of DFF2. These modifications reduce the extra stages between the D flip flops which consequently decreases the number of switching nodes to 7. Power of the switching device can be shown by the equation (5)

$$P_{switching-Design-1} = \sum_{j=1}^{7} C_{Li} f_{in} V_{dd}^2 \quad (5)$$

total load capacitance at the output Q of the proposed design is reduced as compared to conventional design. Due to this delay and power of the circuit is reduced. Saved power from the proposed design can be shown by the formula in (6).

$$P_{switching-saved} = \sum_{i=1}^{12} C_{Li} f_{in} V_{dd}^2 - \sum_{j=1}^{7} C_{li} f_{in} V_{dd}^2 \quad (6)$$

$P_{switching-saved}$ is the power saved which was wasted while switching. Both conventional and proposed design are made using identical width of 3 µm for pMOS and 2 µm for nMOS. Comparing with the conventional design Speed is increased up to 1.3 times and power is saved upto 42%. By reducing the number of stages, switching power is hence reduced.

This design of prescaler saves more than 50% of power in divide by 3 operation and saves only 25% of power in divide by 2 operation in comparison to conventional divide by 2/3 prescaler above 2 Gigahertz frequency.

D. Ultra Low Power TSPC 2/3 Prescaler[6]:

Another design with ultra low power 2/3 prescaler is proposed in figure 6. This is an improvement in the design in section C by adding one more transistor. Transistor ma1 is added between supply voltage and the DFF1's input which is controlled by MC. As DFF1 should be off during the division of frequency by two operation. In this design when logic MC is high in divide by 2 operation ma1 is off which makes DFF1 disconnected from the supply. Switching power as well as short circuit power of DFF1 are completely saved by this arrangement.

In divide by 3 operation when MC goes low, ma1 turns on and power is supplied to DFF1 it works same as the design proposed in section C. In this proposed design DFF1 operates at voltage lower than the supply voltage because some voltage drop is present at ma1 transistor. As operating frequency depends upon supply voltage, proposed design operates at lower frequency then the design in section C.

pMOS transistor M1 is removed which makes it similar to the ETSPC design in [1]. This modification made the operating frequency of this design similar to the design discussed in section C. Power consumed in Dividing frequency by 2 operation is given by (7)

$$P_{2/3\ Design-2} = P_{switching-DFF2} + P_{short-DFF2} \quad (7)$$

Power saves by this design is given by equation (8).

$$P_{2/3\ Design-1} - P_{\frac{2}{3}\ Design-2} = P_{switching-DFF1_{Design}-1} + P_{short-S3-DFF1_{Design}-1} \quad (8)$$

Power saved by this design 2 is 67%.The table III given below compares and analyse the design proposed in section C and D of this paper.

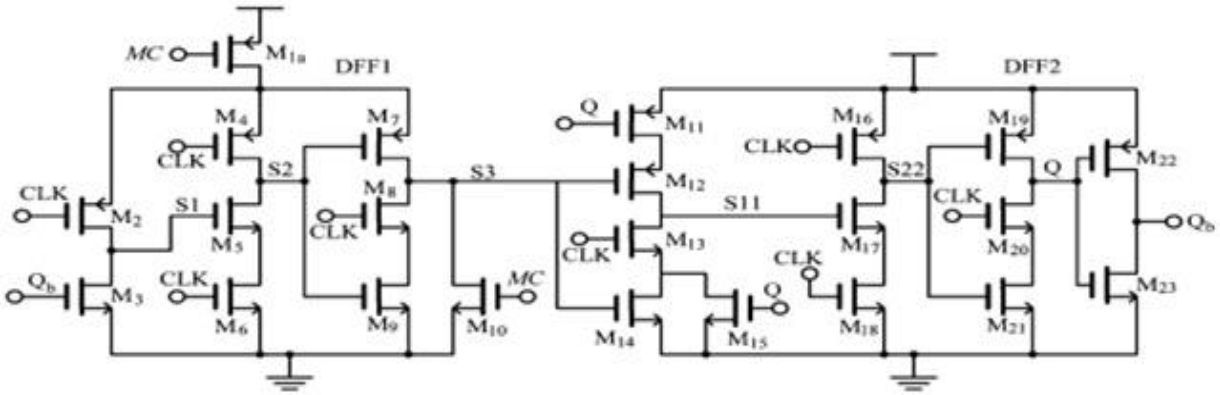

Fig. 6. Proposed Design 2 of TSPC 2/3 Prescaler [6].

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Table IIII. Comparison between Proposed Designs in [1], [2] and [6]

Design Parameters	Prescaler in [1]	Prescaler in [2]	Design-1 Prescaler [6]	Design-2 Prescaler [6]
Process(µm)	0.18	0.18	0.18	0.18
Supply voltage(v)	1.5	1.5	1.8	1.8
Maximum. Frequency (GHz) (Sim/Measured)	5.5	6.7	5.5/4.9	5.5/4.9
Power (mW) (Sim/Measured) Divide-by-2 mode	1.78	1.433	0.923/1.03	0.252/0.306
Power (mW) (Sim/Measured) Divide-by-3 mode	1.643	1.554	0.369/0.445	0.387/0.461

III. CONCLUSION

In this paper various techniques to make divide by 2/3 dual modulus prescalers have been discussed. In total four techniques have been discussed in which two are based on TSPC D flip flop and two are based on ETSPC D flip flop. The above-mentioned circuits can be used for designing frequency dividers in PLL. Many techniques such as device sizing, body biasing can be done to decrease the delay and power of the circuit. In this paper our aim was to find the best 2/3 dual modulus prescaler in terms of delay and power in order to help the designer to select the best 2/3 prescaler for their design specification. From this research it has been found that proposed design of ETSPC based divide by 2/3 dual modulus prescaler using a pass transistor as in [5] is best in terms of power and delay.

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